CHAPTER 11

CRYSTAL FILTER ASSEMBLY M32-3461-01

UNIT 13

CONTENTS LIST

	Paragraphs
Description	1, 2

ILLUSTRATIONS

	Figure No
Passband Response Curves	11.1
Filters Band-pass LSB and USB	11.2
Filters Band-pass DSB, CW, FST	11.3
Crystal Filter Assembly Circuit Diagram	11.4

CHAPTER 11

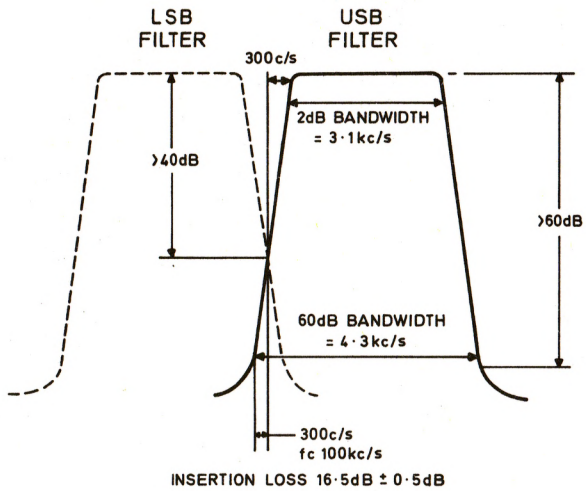
CRYSTAL FILTER ASSEMBLY M32-3461-01

UNIT 13

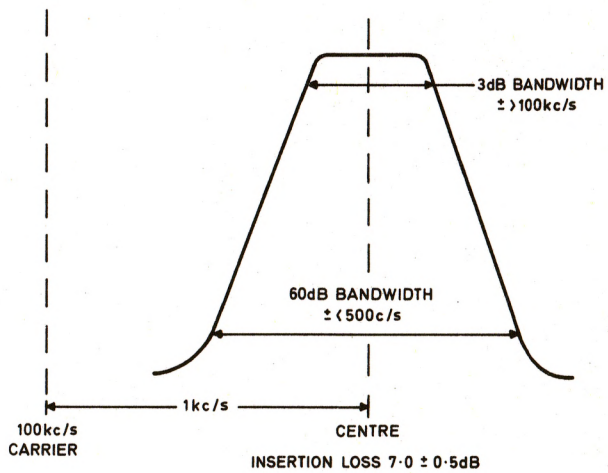
Description

1. The Crystal Filter Assembly contains five crystal band-pass filters, the bandwidth of each being appropriate to a particular mode: lsb, dsb, usb, cw or fst. Four filters are for usb or dsb use and one for lsb. Filters are selected by diode switching in Panel, Filter Switching, Unit 12.

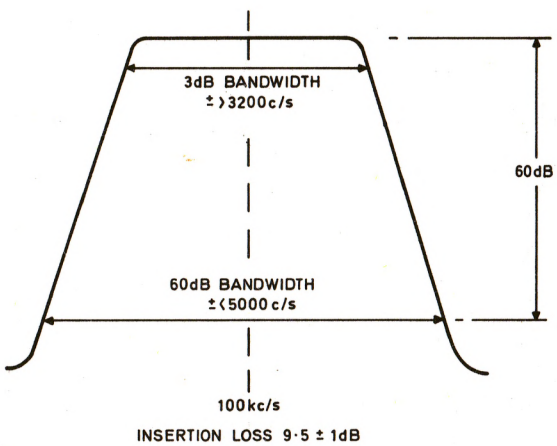
2. The filters are mounted on a plate located by two dowel pins at the bottom and secured by two screws at the top. The assembly includes a 32-way edge connector into which the Filter Switching Panel, unit 13, is plugged. Connections from other sub-assemblies are also by plug and socket. Each filter is hermetically sealed and screwed to the plate. Input and output connections are by soldered terminals.



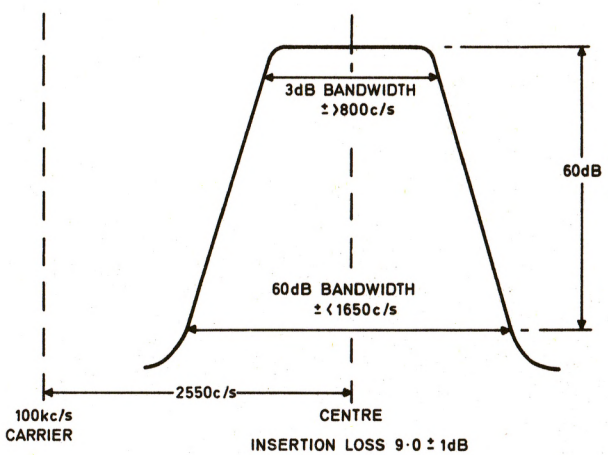
FL1 LSB (5915-99-519-6999)
FL3 USB (5915-99-519-6998)



FL4 CW (5915-99-519-7026)



FL2 DSB (5915-99-519-7024)

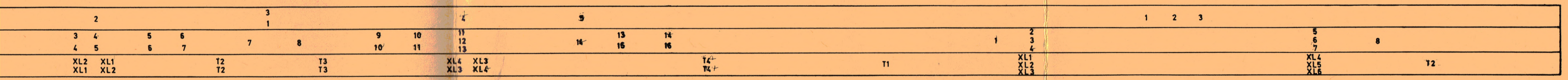


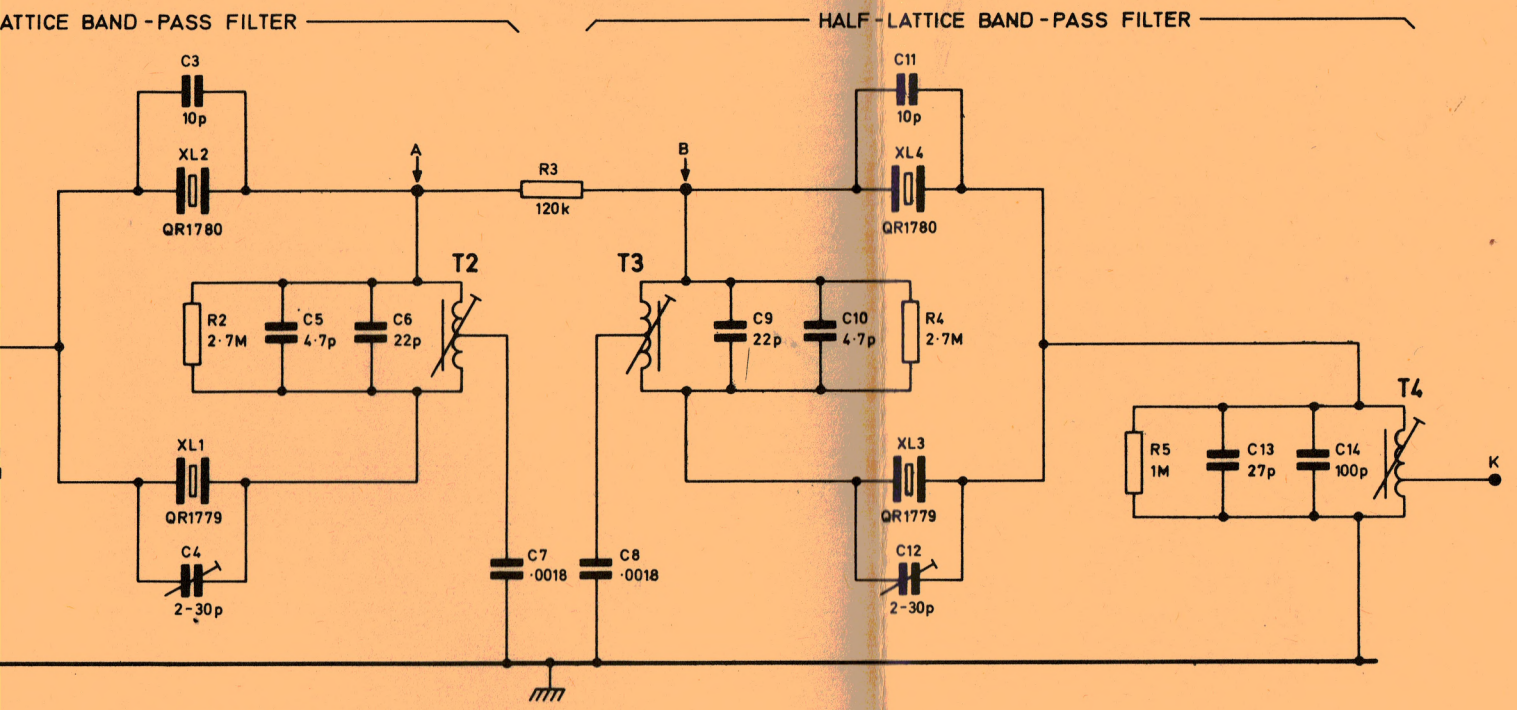
FL5 FST (5915-99-519-7025)

CRYSTAL FILTER PASSBAND RESPONSE CURVES

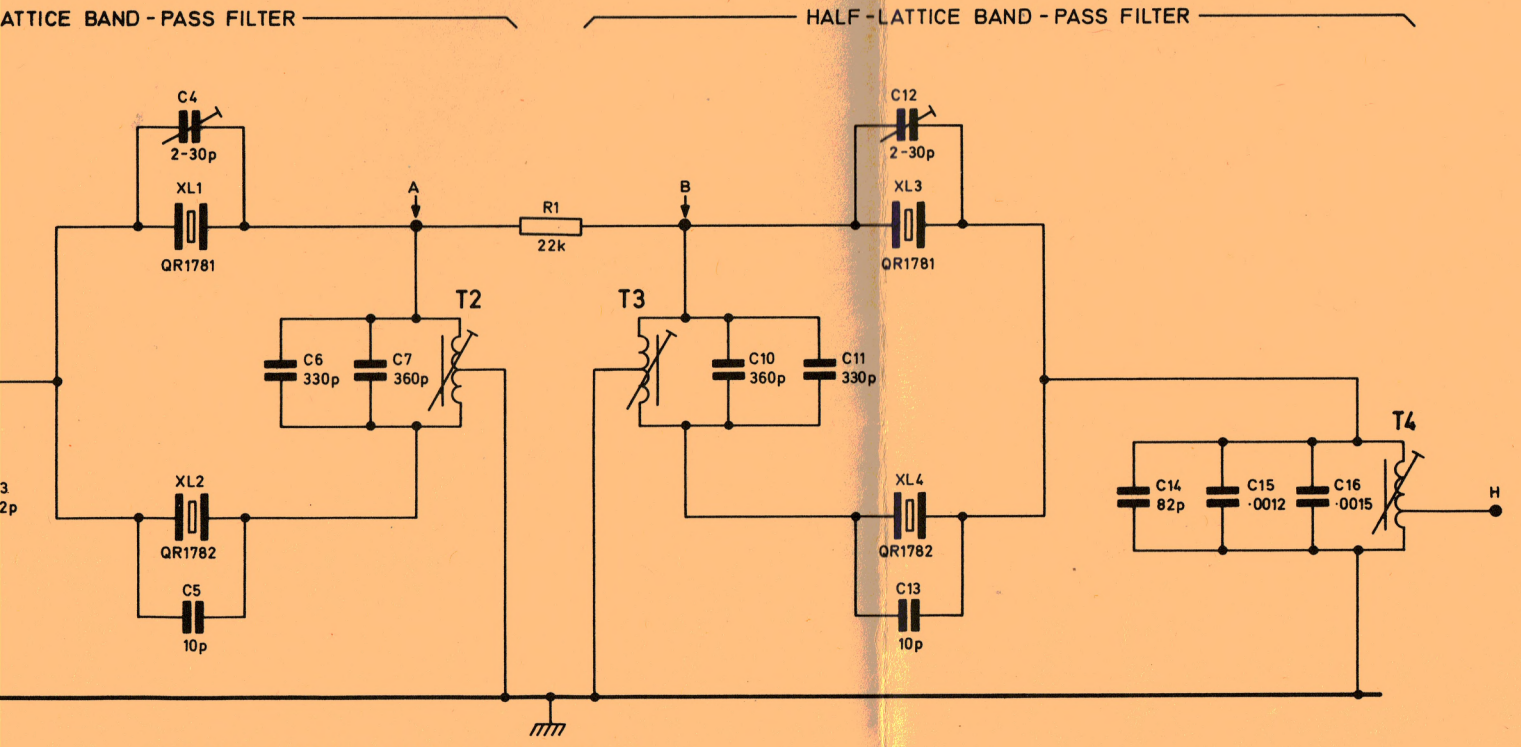
FIG.11·1

| | | |

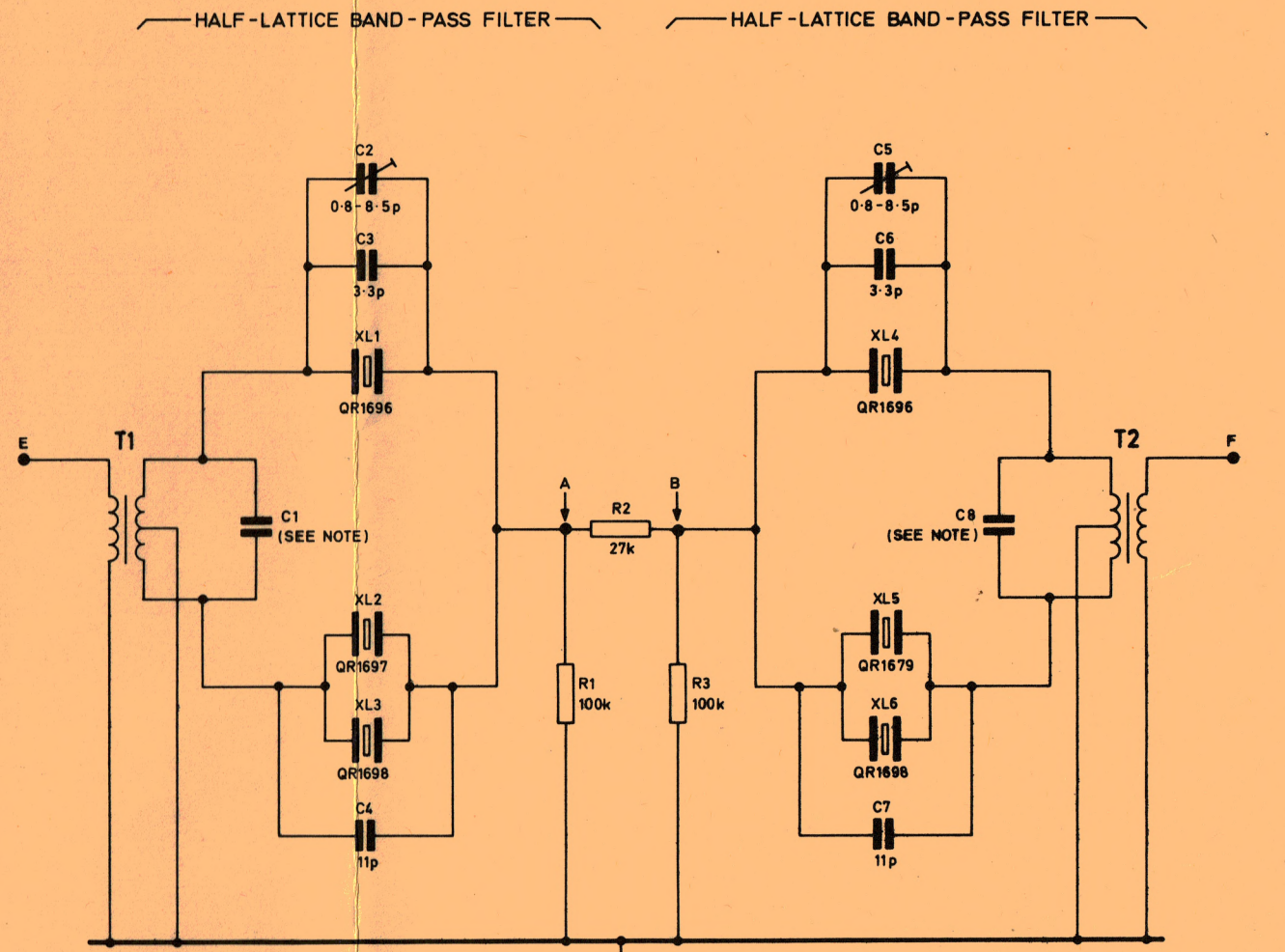




FL2 DSB FILTER (5915-99-519-7024)



FL5 FST FILTER (5915-99-519-7025)



FL4 CW FILTER (5915-99-519-7026)

NOTE. C1 & C8 IN FL4 ARE SELECTED ON TEST AND, IF FITTED ARE EITHER 2·2p, 4·7p OR 6·8p

PANEL FILTERS BANDPASS

FL1 TO FL5

DSB (FL2)	5915-99-519-7024
CW (FL4)	5915-99-519-7026
FST (FL5)	5915-99-520-4052
PART OF SUB-ASSEMBLY 13	CIRCUIT DIAGRAM

MOD RECORD					
1	2	3	4	5	6
7	8	9	10	11	12

FIG. 11·3

| | | |

CRYSTAL FILTER ASSEMBLY
(M32-3461-01)

13

PART OF PANEL FILTER SWITCHING
(5820-99-519-7023)

12

PART OF PANEL FILTER SWITCHING
(5820-99-519-7023)

12

1TS1-8

ER
4PLAV-S)

PANEL
-5)

NIT

PLAU
B

SKTL PLL
4
+30V

DIODE SWITCH

R1
220

PLER
D1
CV7332
R2
15k

PLEQ
6

AMPLIFIER
VT3

PLAU
A
5

(UNIT 1)

DIODE SWITCHES

MR9
FST

MR7
CW

MR3
DSB

MR5
USB

AMPLIFIER
VT2

MR2
LSB

PLL SKTL
15
14
G
FL5-FST
H
T

18
17
E
FL4-CW
F

12
11
J
FL2-DSB
K

9
8
C
FL3-USB
D

2
1
A
FL1-LSB
B

SKTL PLL
22
21

20
19

24
23

27
28

31
32

DIODE SWITCHES
MR10
FST

MR8
CW

MR4
DSB

MR6
USB

MR1
LSB

AMPLIFIER
VT4

PLL SKTL
26
25

30
29

AMPLIFIER
VT1

PLEL
100kc/s USB/DSB
FILTERED I.F. TO
AMPLIFIER I.F. (USB/DSB)
UNIT 10 (10PLJ-32)

PLEM
100kc/s LSB FILTERED I.F.
TO AMPLIFIER I.F. (LSB)
UNIT 11 (11PLK-22)

F
FST FILTER SWITCH
13

D
CW FILTER SWITCH
16

MCW
E
DSB FILTER SWITCH
10

DATA
C
USB FILTER SWITCH
7

DATA
H
LSB FILTER SWITCH
3

CRYSTAL FILTER ASSEMBLY M32-3461-01

SUB-ASSEMBLY 13 CIRCUIT DIAGRAM

FIG. 11·4

CRYSTAL FILTER ASSEMBLY
(M32-3461-01)

PART OF PANEL FILTER SWITCHING
(5820-99-519-7023)

PART OF PANEL FILTER SWIT
(5820-99-519-7023)

(12)

(13)

(12)

1TS1-8

+30V FROM POWER SUPPLY UNIT 14 (14PLAV-S)

PLAU B

SKTL PLL 4 → +30V

DIODE SWITCH

R1 220

PLER D1 CV7332 R2 15k

100kc/s TEST SIGNAL FROM PANEL DEMODULATOR UNIT 7 (7PLF-5) (ALSO CARRIES SWITCHING CURRENT FOR D1)

PLEQ

100kc/s I.F. FROM TUNING UNIT RECEIVER UNIT 2 (2PLEK)

PLAU A

(UNIT 1)

6

5

AMPLIFIER VT3

DIODE SWITCHES

MR9 → FST

MR7 → CW

MR3 → DSB

MR5 → USB

AMPLIFIER VT2

MR2 → LSB

PLL SKTL

15 14

18 17

12 11

9 8

2 1

FL5-FST G H

FL4-CW E F

FL2-DSB J K

FL3-USB C D

FL1-LSB A B

SKTL PLL

22 21

20 19

24 23

27 28

31 32

DIODE SWITCHES

MR10 → FST

MR8 → CW

MR4 → DSB

MR6 → USB

MR1 → LSB

AMPLIFIER VT4

AMPLIFIER VT1

USB	FST	F	FST FILTER SWITCH	13
	CW	D	CW FILTER SWITCH	16
	DSB & MCW	E	DSB FILTER SWITCH	10
	SSB & DATA	C	USB FILTER SWITCH	7
LSB	SSB DATA	H	LSB FILTER SWITCH	3

30V SWITCHING POTENTIAL FROM SYSTEM SWITCHES 1SD1F & 1SF1F

LSB NOT AVAILABLE WHEN EITHER DSB OR MCW SELECTED ON USB

SEE FIGURE 12-3 FOR FULL SWITCHING DETAILS

CRYSTAL FILTER
SUB-ASSEMBLY 13

CHAPTER 12

PANEL FILTER SWITCHING 5820-99-519-7023

UNIT 12

CONTENTS LIST

	Paragraphs
Introduction	1, 2
Physical Description	3, 4
Electrical Description	5 - 16

ILLUSTRATIONS

	Figure No
Panel Filter Switching Block Diagram	12.1
Panel Filter Switching Component Layout	12.2
Panel Filter Switching Circuit Diagram	12.3

CHAPTER 12

PANEL FILTER SWITCHING 5820-99-519-7023

UNIT 12

Introduction

Figure 12.1

1. 100 kHz i.f. from the 1 MHz I.F. Amplifier, unit 20, is fed to the Panel Filter Switching where it is switched through selected filters in Crystal Filter Assembly, unit 13, to produce 100 kHz filtered i.f. for two receiver channels. One channel is for usb, dsb, cw or fst reception and the other for lsb reception.

2. The incoming signal is fed to channel amplifiers VT2, VT3 and routed by diode switches through the appropriate filters to output amplifiers VT1, VT4. The diode switches are controlled by -30 V switching potential from the front panel system switches.

Physical Description

3. Unit 12 is a plug-in printed wiring board 7.2 inches by 5.5 inches. A finger pull facilitates removal and slotted guides assist location of the board into its socket. Rubber pads on the printed-wiring side prevent the board from being inserted in the wrong position.

4. The board is screened on both sides. The screen on the component side is partitioned to prevent radiation between channels and between the input and output halves of the switch. The screens are earthed by the mounting pillars.

Electrical Description

Figure 12.3

5. The incoming signal from 20PLP3 via 2PLEK, 13PLEQ to 12PLL6 is applied simultaneously to the bases of amplifiers, VT2, VT3. The output of VT3 provides the usb, dsb path and that of VT2, the lsb path. The usb, dsb signal may be fed to one of four crystal filters depending on its supplementary characteristic. It is then fed via a further amplifier stage VT4 to the Amplifier I.F. (100 kHz) unit 10. VT2 feeds the lsb signal via the lsb crystal filter and amplifier stage VT1 to the Amplifier I.F. (100 kHz) unit 11.

6. The signal is routed to the correct filter by one diode switch before and one diode switch after each crystal filter. There are five crystal filters and therefore five pairs of switching diodes. The operation of each pair of diodes is identical and that of only one pair, MR5, MR6, is described.

7. In the USB position of the front panel switch, the signal path from VT3 collector to VT4 base is via MR5, crystal filter FL3 and MR6.

8. The signal is largely attenuated if the two diodes are biased into their non-conducting, high impedance condition. Alternatively, the signal can pass through the circuit if the diodes are biased into their conducting, low-impedance condition.

9. To bias the diodes into conduction -30 V is applied to the appropriate switching line. This is applied to MR5 via the current controlling resistor R31. Filtering is provided by C21, R32, C24 and R35, and the return to chassis is via L3. R37 is the current controlling resistor for MR6 and filtering is provided by C26, R36, C24. The return path to chassis is via L4.

10. When the -30 V on the switching line is removed MR5, MR6 are reverse biased by +30 V via R34.

11. It is necessary to terminate the crystal filter in 2.2 kohms. At the input this is achieved by the low output impedance amplifier VT3 and a series resistor of 2.2 kohms, R29. At the output it is provided by R37 in parallel with R46, R47, the biasing resistor of VT4. C19, C25 are d.c. blocking capacitors.

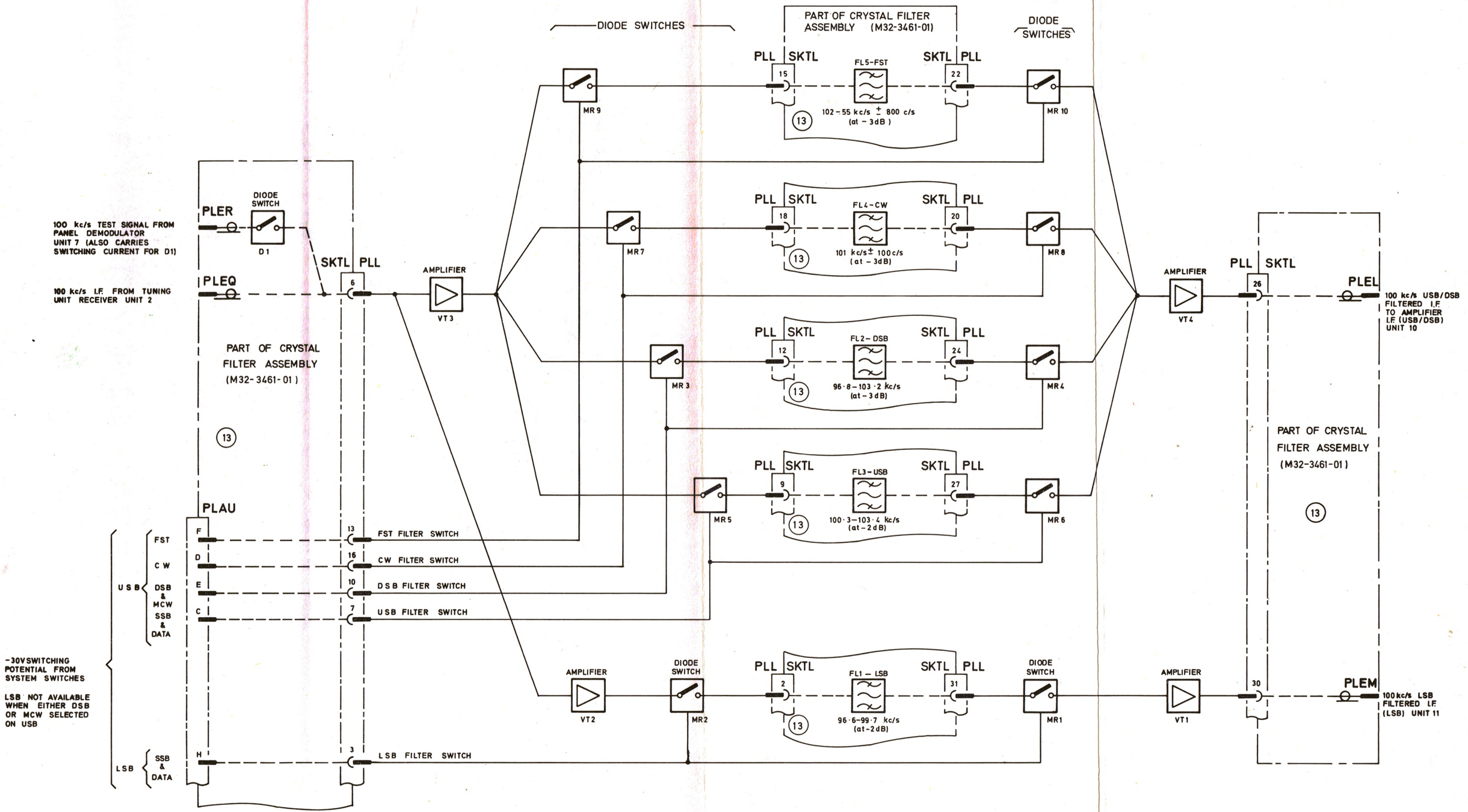
12. Input amplifiers VT2, VT3 share biasing resistors R27, R28. T2, T3 provide voltage feedback which ensures steady gain and low output impedance at the collector. The transistors are low noise, high gain devices.

13. Output amplifiers VT1, VT4 have their own biasing resistors. The gain is also controlled by negative voltage feedback provided by T1, T4. Outputs are taken from the centre-tapped secondary windings of these transformers.

14. C40, C43 and C4, C30 prevent parasitic high frequency oscillation in the input and output amplifiers respectively.

15. Only one of the four circuits in the usb/dsb channel can be in operation. The lsb channel can operate simultaneously with the usb, cw or fst filter circuits. It can also operate with the usb/dsb channel switched off, when the usb/dsb channel cannot be made operational.

16. To equalise the insertion loss of the filters the dsb circuit is attenuated by R22, R24, R25 and the fst circuit by R57, R59, R61.



PANEL FILTER SWITCHING 5820-99-519-7023

SUB-ASSEMBLY 12 BLOCK DIAGRAM

FIG.12·1

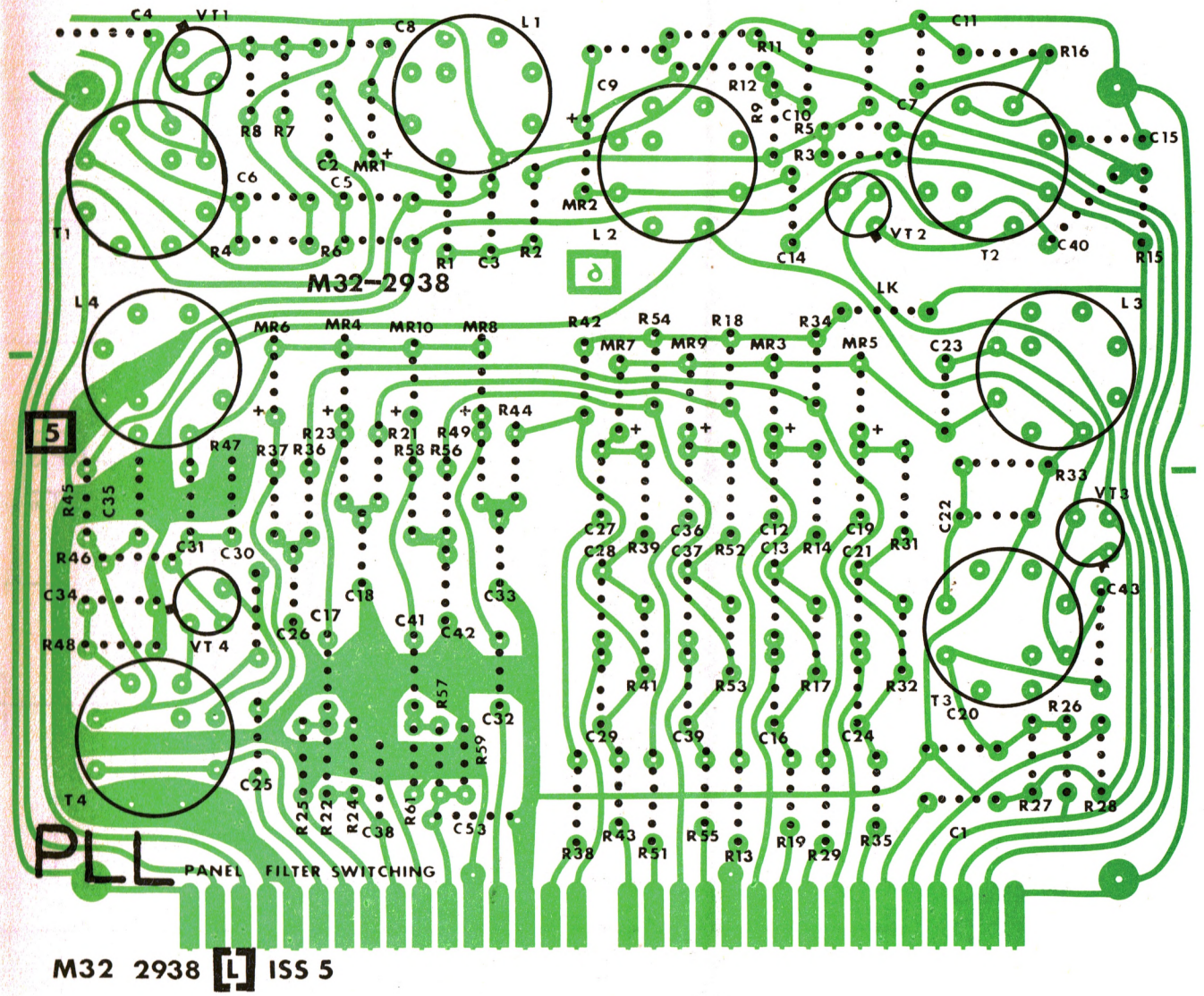


FIG. 12.2 PANEL FILTER SWITCHING COMPONENT LAYOUT

DIODE SWITCHES

DIODE SWITCHES

PART OF CRYSTAL FILTER ASSEMBLY (M32-3461-01)

AMPLIFIER

AMPLIFIER

PART OF CRYSTAL FILTER ASSEMBLY (M32-3461-01)

PLL

13

FL5-FST 102·55 kc/s ± 800 c/s (at − 3dB)

FL4-CW 101 kc/s ± 100 c/s (at − 3dB)

FL2-DSB 96·8 − 103·2 kc/s (at − 3dB)

FL3-USB 100·3 − 103·4 kc/s (at − 2dB)

FL1-LSB 96·6 − 99·7 kc/s (at − 2dB)

L3 L4 L1

MR9 MR10 MR7 MR8 MR3 MR4 MR5 MR6 MR1

U3053

R52 3·3k R53 470 R54 100k R55 150 R56 470 R57 1·8k R58 8·2k R59 5·6k R61 6·8k

R39 3·3k R41 470 R42 100k R43 150 R44 470 R45 1k R46 18k R47 3·9k R48 2·2k

R14 3·3k R17 470 R18 100k R19 150 R21 470 R22 1·8k R23 8·2k R24 5·6k R25 6·8k

R31 3·3k R32 470 R34 100k R35 150 R36 470 R37 8·2k R6 1k R7 18k R8 3·9k

R38 2·2k R49 8·2k R13 2·2k R29 2·2k R11 2·2k R1 8·2k R2 470 R4 2·2k

C36 C41 C27 C32 C12 C17 C19 C25 C9 C2 C31 C8 C7 C39 C28 C29 C16 C18 C33 C35 C30 C34 C13 C21 C24 C26 C37 C42 C5 C4 C6 C3

0·1

C53 C38 68p

T4 T1

VT4 VT1 A1505

+30V

PLEL PLEM

100 kc/s USB/DSB FILTERED I.F. TO AMPLIFIER I.F. (USB/DSB) UNIT 10 (10 PLJ - 32)

100 kc/s LSB FILTERED I.F. TO AMPLIFIER I.F. (LSB) UNIT 11 (11 PLK - 32)

MOD RECORD					
1	2	3	4	5	6
7	8	9	10	11	12

PANEL FILTER SWITCHING 5820-99-519-7023

SUB-ASSEMBLY 12

CIRCUIT DIAGRAM

FIG.12·3

| | | |

CHAPTER 13

AMPLIFIER INTERMEDIATE FREQUENCY (100 KHZ)

5820-99-519-7031

UNITS 10 AND 11

CONTENTS LIST

	Paragraphs
Introduction	1 - 4
Physical Description	5
Electrical Description	6 - 17

ILLUSTRATIONS

	Figure No
Amplifier Intermediate Frequency Block Diagram	13.1
Amplifier Intermediate Frequency Component Layout	13.2
Amplifier Intermediate Frequency Circuit Diagram	13.3

CHAPTER 13

AMPLIFIER INTERMEDIATE FREQUENCY (100 KHZ)

5820-99-519-7031

UNITS 10 AND 11

Introduction

Figure 13.1

1. Unit 10 is used for usb, dsb operation. Unit 11 is used for lsb operation. Each amplifier accepts an input at 100 kHz from the appropriate sideband filter and provides up to 70 dB of amplification. The output is applied to Panel Demodulator, Unit 6.

2. Automatic gain control is employed and maintains zero error output over the A.G.C. range . Up to 80 dB of attenuation can be applied in two stages. Firstly, an error output of up to 6 dB from the band-pass tuned amplifier at PLJ, PLK10 is applied to the Panel Automatic Gain Control, Unit 8 or 9 which produces the necessary d.c. bias via PLJ, PLK16 to provide 74 dB of attenuation. The error output is then reduced to zero by incorporating a further 6 dB of attenuation in a 'Forward A.G.C.' stage, so called because it is outside the A.G.C. feedback loop.

3. A squelch circuit may be switched in or out by the SQUELCH switch on the front panel. When the SQUELCH switch is to IN the signal is attenuated by approximately 30 dB if it should fall below a predetermined threshold level. This reduces operator fatigue when working with a strong signal. During no-signal periods the Receiver output is reduced and noise reduced to a negligible level.

4. VT1 to VT4 form a four-stage amplifier with tuned filters between each stage. A.G.C. is applied to the first three stages. VT4 is a voltage feedback amplifier and provides a low impedance output to operate the external A.G.C. circuits and the forward A.G.C. circuit. Forward A.G.C. is applied to MR10 which provides the necessary attenuation between VT4 and VT5. MR11 provides the optional squelch facility. VT5 provides a low-impedance output for ssb operation and a high impedance output for dsb operation.

Physical Description

5. Each unit is a plug-in printed wiring board 7.2 inches by 5.5 inches. A finger pull facilitates removal and slotted guides assist location of the board. Rubber pads on the printed-wiring side prevent it being inserted in the wrong position. The board is screened on both sides. The screens are earthed by the mounting pillars.

Electrical Description

Figure 13.3

6. The 100 kHz input from unit 13 appears at PLJ, PLK32. R1 provides the fixed source impedance which is necessary for the A.G.C. response.

7. The A.G.C. voltage input from Unit 8 or 9 at PLJ, PLK16 is applied, via the diode resistor network MR1, MR2, R2, R3, R4 to the shunting diode MR3.

8. The slope impedance of a diode varies with the current passing through it. Thus $R = \frac{25}{I}$ where R is diode resistance in ohms and I is diode current in mA.

9. Using this principle VT1 base can be controlled by shunting the input impedance by MR3. By controlling this shunting in conjunction with fixed source impedance R1, a precise control of the input to the amplifier is achieved.

10. MR3 current depends on the A.G.C. voltage which is controlled by R2 to R5 and MR1, MR2. MR2 will not conduct until approximately 0.5 V is developed across R4 and MR1 will not conduct until approximately 0.5 V is developed across R3. So the current in MR3, and therefore its shunting effect, is precisely controlled. R43 provides the main load on the A.G.C. circuit. C31 reduces interstage feedback via the A.G.C. line.

11. VT1 is biased by R6, R7, R13. Current control is provided by R8, R9 decoupled by C6. R8 provides feedback which, with collector impedance, controls the gain. The collector load is a pair of capacitively-coupled tuned circuits, the output being transformer coupled to the next stage.

12. The second and third stages VT2, VT3 are identical to the first, except as follows:-

(a) The first stage is required to handle higher signal levels than the other two stages when the Receiver is receiving strong signals. To prevent it producing intermodulation products MR3 carries a higher d.c. current than the other A.G.C. diodes MR6, MR9.

(b) The Q of the tuned circuits is increased by using larger shunt resistors, 22 kohms compared with 18 kohms in the first stage. This also increases the gain of VT2, VT3.

(c) Inter-stage coupling is increased. The first pair is slightly less than critically coupled and the other two slightly more than critically coupled, to give a flat response over a bandwidth of $\pm$ 3.4 kHz.

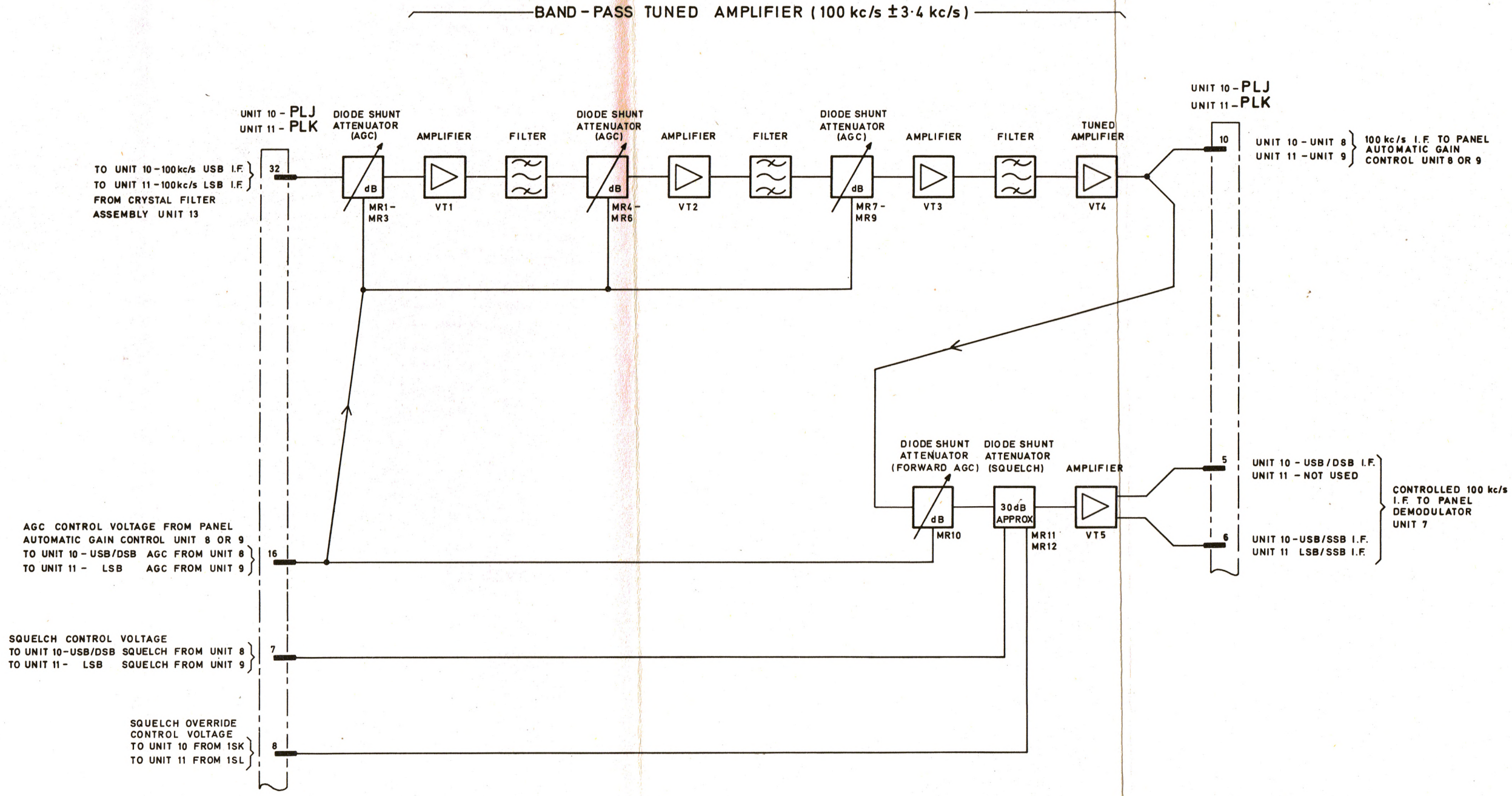
13. Amplifier VT4 is not controlled by A.G.C. The low-impedance output level varies by 6 dB for a 120 dB change in signal level at the aerial. This 6 dB is applied to unit 8 or 9 and produces the required A.G.C. voltage.

14. The forward A.G.C. attenuates the reference signal by 6 dB and then by a further 6 dB when the input level is increased to maximum, corresponding to 120 dB change at the antenna, which removes all variation in output due to variation in signal strength. The circuit comprises R48, R50, R51, C44, MR10 and T8. The resistance of MR10 is controlled by the current passing through it which, when no A.G.C. operates, is controlled by fixed resistor R50 and produces 6 dB of attenuation. As the signal level rises A.G.C. becomes operative and additional current flows through MR10 via R51. This reduces the resistance of MR10 and therefore increases its shunting effect. At full A.G.C. the circuit thus applies 12 dB of attenuation.

15. The squelch function is performed by MR11. With no inhibiting bias appearing via R57, MR11 is biased into conduction by R52, T53 and shunts the signal path thereby providing approximately 30 dB of attenuation. Thus, the circuit is squelched. To return to normal operation MR11 must be reverse biased, either from the A.G.C. circuit or from the SQUELCH switch on the front panel. When the switch is set to OUT, -30 V is applied to MR11 via R57, R54 thus reverse-biasing it and MR12 prevents the -30 V appearing at PLJ, PLK7.

16. VT5 produces two outputs. The low-impedance emitter output supplies the ssb detector at a low signal level of approximately 80 mV. The high-impedance collector output supplies the dsb detector at a high signal level of approximately 215 mV.

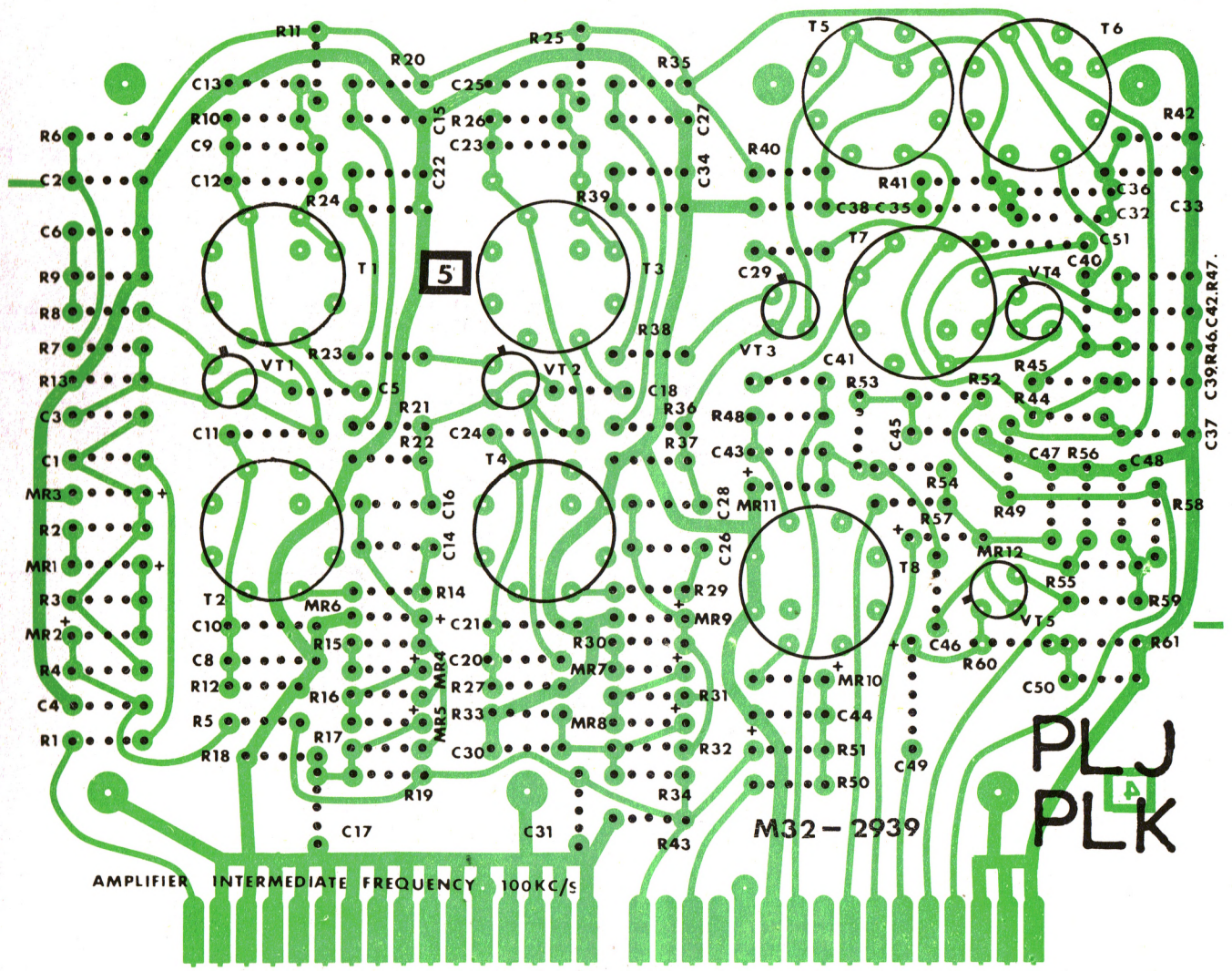
17. When on usb/dsb both the ssb and dsb outputs, from unit 10, are used. When on lsb the ssb output only, from unit 11, is used.



AMPLIFIER INTERMEDIATE FREQ. 5820-99-519-7031

SUB-ASSEMBLIES 10 & 11 — BLOCK DIAGRAM

FIG. 13·1



M32-2939 [L] ISS 5

FIG. 13.2 AMPLIFIER INTERMEDIATE FREQUENCY COMPONENT LAYOUT

BR 4147 (5) A
Original

BAND-PASS TUNED AMPLIFIER (100 kc/s ±3·4 kc/s)

ATOR (A.G.C.) — AMPLIFIER — FILTER — DIODE SHUNT ATTENUATOR (A.G.C.) — AMPLIFIER — FILTER — DIODE SHUNT ATTENUATOR (A.G.C.) — AMPLIFIER — FILTER

+30V — +30V (NOM) — C37 0·1 — (Y) — +30V (NOM) — R6 27k — C2 0·1 — (Z) — R7 12k — C3 ·01 — R3 10k — R4 27k — MR2 CV7332 — (Z) — C4 ·01 — R5 1·8k — R13 27k — (Z) — C5 10p — T1 — +30V (NOM) — R11 4·7k — C13 0·1 — (Z) — C12 47p — C9 680p — R10 18k — VT1 A1505 — R8 180 — R9 10k — C6 0·1 — (Z) — C11 68p — T2 — C8 47p — C10 680p — R12 18k — (Z) — (Z) — MR6 CV7332 — C14 ·01 — R14 3·9k — MR4 CV7332 — R15 8·2k — R16 56k — MR5 CV7332 — R17 56k — R18 5·6k — C17 ·01 — R19 5·6k — +30V (NOM) — R20 27k — C15 0·1 — (Z) — C16 ·01 — R21 12k — R22 27k — (Z) — +30V (NOM) — T3 — R25 4·7k — C25 0·1 — (Z) — C23 680p — R26 22k — C18 10p — VT2 A1505 — R23 150 — R24 10k — C22 0·1 — (Z) — C24 100p — C20 10p — T4 — C21 680p — R27 22k — (Z) — (Z) — MR9 CV7332 — C26 0·1 — R29 3·9k — MR7 CV7332 — R30 82k — R31 56k — R32 56k — MR8 CV7332 — R33 5·6k — C30 0·1 — R34 5·6k — +30V (NOM) — R35 27k — C27 0·1 — (Z) — C28 ·01 — R36 12k — T5 — +30V (NOM) — R40 4·7k — C38 0·1 — (Z) — C35 680p — R41 22k — C29 10p — VT3 A1505 — R37 27k — (Z) — R38 120 — R39 10k — C34 0·1 — (Z) — C36 100p — C32 10p — T6 — C33 680p — R42 22k — (Y) — TO C40

kc/s ±3·4 kc/s) — IED AMPLIFIER — DIODE SHUNT ATTENUATOR FORWARD A.G.C. — DIODE SHUNT ATTENUATOR (APPROX 30dB SQUELCH) — AMPLIFIER

+30V (NOM) — R44 2·2k — T7 — C39 0·1 — (Y) — C51 47p — C41 ·01 — VT4 A1505 — R47 10k — C42 0·1 — (Z) — TO PLJ/PLK 10 — T8 — R48 3·9k — C43 ·01 — MR10 CV7332 — C44 1 — (Z) — R51 1k — R50 27k — -30V — +30V — R52 10k — R53 47k — C45 0·1 — (Y) — MR11 CV7332 — (Z) — R54 27k — C47 0·1 — (Y) — MR12 CV7332 — R57 10k — C46 680p — +30V — R58 1·8k — R55 68k — R59 2·2k — C48 0·1 — (Y) — VT5 A1505 — C49 6·8 — R56 33k — R60 820 — R61 2·2k — C50 0·1 — (Y)

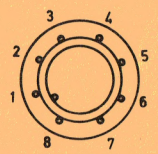
UNIT 10 – PLJ
UNIT 11 – PLK

FROM C41 — 10 — UNIT 10 – 100 kc/s I.F. (TO 8 PLG-3) — UNIT 11 – 100 kc/s I.F. (TO 9 PLG-3) — } 100 Kc/s TO I.F. TO PANEL AUTOMATIC GAIN CONTROL UNIT 8 OR 9

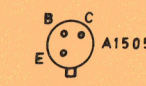
5 — UNIT 10 – USB/DSB I.F. (TO 7 PLF-22) — UNIT 11 – NOT USED

6 — UNIT 10 USB/SSB I.F. (TO 7 PLF-16) — UNIT 11 USB/SSB I.F. (TO 7 PLF-14) — } CONTROLLED 100 kc/s I.F. TO PANEL DEMODULATOR UNIT 7

UNIT 10		UNIT 11	
PLJ		PLK	
PIN	DESTINATION	PIN	DESTINATION
1-3, 11, 17-31	EARTH	1-3, 11, 17-31	EARTH
4	1TS1-4 & 14 PLAV-S	4	1TS1-4 & 14 PLAV-S
5	7 PLF-22	5	———
6	7 PLF-16	6	7 PLF-14
7	8 PLG-29	7	9 PLH-29
8	1SK	8	1SL
10	8 PLG-3	10	9 PLH-3
14	1TS2-6 & 14 PLAV-Y	14	1TS2-6 & 14 PLAV-Y
16	8 PLG-8	16	9 PLH-8
32	13 PLEL	32	13 PLEM



T1 – T8



VT1 – VT5

BASE VIEWS

MOD RECORD					
1	2	3	4	5	6
7	8	9	10	11	12

AMPLIFIER INTERMEDIATE FREQUENCY (100 kc/s) 5820-99-519-7031

SUB-ASSEMBLIES 10 & 11

CIRCUIT DIAGRAM

FIG. 13·3

RES	43 1 49 2 45 46 3 44 4 5 47 6 7 13 11 10 48 8 9 51 50 12 52 53 54 14 57 15 16 55 17 19 18 20 56 58 21 59 22 60 61 25 26 23 24 27
CAP	31 40 1 37 2 4 3 42 41 51 5 39 12 9 6 13 11 8 44 43 10 45 14 47 46 15 16 17 18 50 48 49 23 25 24 22 20 21
MISC.	MR3 MR1 MR2 T7 VT4 T1 VT1 T8 MR10 T2 MR11 MR12 MR6 MR4 MR5 VT5 T3 VT2 T4

BAND-PASS TUNED AMPLIFIER (100 kc/s ±3·4 kc/s)

DIODE SHUNT ATTENUATOR (AGC) — AMPLIFIER — FILTER — DIODE SHUNT ATTENUATOR (AGC) — AMPLIFIER — FILTER

UNIT 10 - PLJ
UNIT 11 - PLK

+30V FROM POWER SUPPLY UNIT 14 (14 PLAV-S) — 1TS1-4 — 4

11

17 TO 31

1

2

3

(UNIT-1)

-30V FROM POWER SUPPLY UNIT 14 (14 PLAV-Y) — 1TS2-6 — 14 — -30V

TO UNIT 10-100 kc/s USB I.F. (FROM 13 PLEL)
TO UNIT 11-100 kc/s LSB I.F. (FROM 13 PLEM)
FROM CRYSTAL FILTER ASSEMBLY UNIT 13 — 32

+30V — R49 820 — C37 0·1 (Y) — +30V (NOM)

(Z) — (Y)

MR3 CV7332 — C1 ·01 — R1 3·9k — MR1 CV7332

R2 1·8k — R3 10k — R4 27k — MR2 CV7332

C4 ·01 (Z) — R5 1·8k

+30V (NOM) — R6 27k — C2 0·1 (Z) — R7 12k — C3 ·01 — R13 27k (Z)

T1 — C5 10p — C12 47p — C9 680p — R10 18k — +30V (NOM) R11 4·7k — C13 0·1 (Z)

VT1 A1505 — R8 180 — R9 10k — C6 0·1 (Z)

C11 68p — T2 — C8 47p — C10 680p — R12 18k (Z)

(Z) — MR6 CV7332 — C14 ·01 — R14 3·9k — MR4 CV7332

R15 8·2k — R16 56k — R17 56k — MR5 CV7332

+30V (NOM) — R20 27k — C15 0·1 (Z) — R21 12k — C16 ·01

T3 — C18 10p — C23 680p — R26 22k — +30V (NOM) R25 4·7k — C25 0·1 (Z)

VT2 A1505 — R22 27k (Z) — R23 150 — R24 10k — C22 0·1 (Z)

C24 100p — C20 10p — T4 — C21 680p — R27 22k (Z)

(Z) — R18 5·6k — C17 ·01

R19 5·6k

(100 kc/s ±3·4 kc/s)

TUNED AMPLIFIER — DIODE SHUNT ATTENUATOR FORWARD A.G.C. — DIODE SHUNT ATTENUATOR (APPROX 30dB SQUELCH) — AMPLIFIER

+30V (NOM) — R44 2·2k

T7 — FROM T6-6 — R45 15k — C40 ·01 — C39 0·1 (Y) — C51 47p — C41 ·01

VT4 A1505 — R46 47k — R47 10k — C42 0·1 (Z)

TO PLJ/PLK 10

T8 — R48 3·9k — MR10 CV7332 — C44 1 (Z) — C43 ·01

+30V — R52 10k — R53 47k — C45 0·1 (Y)

MR11 CV7332 (Z) — R54 27k — C47 0·1 (Y)

MR12 CV7332 — R57 10k

R51 1k — R50 27k — -30V

+30V — R58 1·8k

R55 68k — R59 2·2k — C48 0·1 (Y)

C46 680p — VT5 A1505 — C49 6·8

R56 33k — R60 820 — R61 2·2k — C50 0·1

(Y)

AGC CONTROL VOLTAGE (0 TO -17V) FROM PANEL AUTOMATIC GAIN CONTROL UNIT 8 OR 9
TO UNIT 10-USB/DSB AGC (FROM 8 PLG-8)
TO UNIT 11-LSB AGC (FROM 9 PLH-8)

SQUELCH CONTROL VOLTAGE
(+2V SQUELCH ON, -19 V SQUELCH OFF)
FROM PANEL AUTOMATIC GAIN CONTROL UNIT 8 OR 9
TO UNIT 10-USB/DSB SQUELCH (FROM 8 PLG-29)
TO UNIT 11-LSB SQUELCH (FROM 9 PLH-29)

-30V FROM POWER SUPPLY UNIT 14 (14 PLAV-Y) — 1TS2-11 — IN — OUT — SQUELCH (1SK TO UNIT 10, 1SL UNIT 11)

16 — R43 1k — C31 ·047 (Z) — A.G.C.

7

8

FROM C41 — 10 — 5 — 6

UNIT 10 - PLJ
UNIT 11 - PLK

MOD RECORD					
1	2	3	4	5	6
7	8	9	10	11	12

AMPLIFIER I
SUB-ASSEMBLIE

CHAPTER 14

PANEL DEMODULATOR 5820-99-519-7029

UNIT 7

CONTENTS LIST

	Paragraphs
Introduction	1 - 4
Physical Description	5, 6
Electrical Description	7 - 12

ILLUSTRATIONS

	Figure No
Panel Demodulator Diagram	14.1
Panel Demodulator Component Layout	14.2
Panel Demodulator Circuit Diagram	14.3 A, B

CHAPTER 14

PANEL DEMODULATOR 5820-99-519-7029

UNIT 7

Introduction

Figure 14.1

1. I.F. inputs from Units 10 and 11 are demodulated in the Panel Demodulator to provide a.f. outputs for Amplifier Audio Frequency, unit 5. Separate but similar circuits for usb and lsb signals each comprise a detector and a two stage a.f. amplifier which provides low pass filtering, diode limiting to remove noisy spikes, and an emitter follower output.

2. Demodulation is effected by an envelope detector for dsb reception and by balanced modulators for ssb reception. The re-insertion carrier frequency of 100 kHz for the balanced modulators is obtained from the Synthesiser. The dsb or ssb input to the upper sideband a.f. amplifier is switched by MR5, MR9 which may be considered as a single pole change over switch controlled by RECEIVE USB/DSB switching on the front panel.

3. On dsb and mcw, MR9 is closed and MR5 open. On all other modes MR9 is open and MR5 closed. MR10 operates at the same time as MR5 to switch the 100 kHz carrier to the ssb demodulators.

4. A 100 kHz test signal is switched to Unit 13 via PLF5 by MR17 when the METERING switch on the front panel is set to IF TEST ON DSB - 100 kHz.

Physical Description

5. Unit 7 is a plug-in printed wiring board 7.2 inches by 5.5 inches. A finger pull facilitates removal and slotted guides assist location into its socket. Rubber pads on the printed wiring side prevent it being mounted in the wrong position. The screen on each side is earthed by its mounting pillars.

6. Three preset potentiometers, adjusted during initial setting-up, are mounted on the panel. They are accessible through holes in the front screen.

Electrical Description

Figure 14.3A, B

7. The usb and lsb channels are similar in action, but diode switching enables a dsb signal to be routed through the usb channel when required. Only the usb channel is described.

8. The i.f. signal from Amplifier Intermediate Frequency (100 kHz), unit 10 appears at PLF16 and is applied across the balanced modulator MR1-4, R2-5. The 100 kHz input from the Synthesiser at PLF9 is passed via MR10 switching circuit to amplifier VT5 which supplies T2. The centre tapped secondary of T2 provides the re-insertion input to the balanced modulator via R1, R6.

9. The resultant output, at audio frequency, is amplified by VT1, for low pass filtering in the sideband filter L1, C8, C10 and further amplified by VT2. The output from VT2 passes to a limiter circuit, the level of which is set by R27, R29. Close-tolerance resistors R26, R28 divide the level equally between MR6 and MR7. Any output voltage from VT2 which has a peak amplitude greater than the reference level across the diodes is symmetrically limited. VT3 is an emitter follower which provides a.f. outputs for the Amplifier Audio Frequency, unit 5 and for monitoring.

10. During ssb, cw, fst and DATA operation, -30 V is applied to PLF26 and PLF7. This allows diodes MR5 and MR10 to conduct. MR10 allows the 100 kHz carrier from the Frequency Synthesiser to pass, via amplifier VT5, to the ssb detector. MR5 allows the demodulated signal output from the ssb detector to pass to VT1. Under this condition there is no -30 V on PLF19, and MR9 is non-conducting.

11. During dsb or mcw operation, the -30 V is removed from PLF26 and PLF7, thus applying reverse bias to MR5 and MR10 via R10 and R57 respectively, so that these both present a high degree of attenuation to the signals. Under these conditions -30 V is applied to PLF19, so causing MR9 to conduct and present a low-impedance path to the signal from the dsb detector to VT1 base.

12. MR18, MR21 protect VT3, VT8 from accidental damage without affecting their normal operation. For example, if unit 7 is unplugged with power on C17, C49 will be charged to about 20 V and will retain this charge for some time. Whether power is on or not, if the board is then plugged in PLP3, 2 or PLP30, 31 can be connected before other contacts so that VT3 or VT8 base-emitter circuit provides a discharge path for C17 or C49 which could damage the transistor. MR18, MR21 provide easier discharge paths.

B.R.4147 (5) A
Original

94 57 58 59 36 37 55 38 54 56 53 39 40 41 50 51 52 46 47 48 49 43 42 96 RV2 61 1 66 6 62 2 64 3 63 4 65 5 67 7 8 60 9 44 10 45 11 3 2 26 36 1 53 34 33 20 21 24 32 22 30 31 23 28 29 27 25 17 MR10 VT4 T1 VT5 MR8 T2 MR20 MR13 MR11 MR1 MR4 MR12 MR2 MR14 MR3 MR19 MR5 MR9

AMPLIFIER

METERING RECTIFIER

PLF 17 1SB2F-11 — METERING TO 1M1 (FREQ. CH. DRIVES -100kc/s)

5 (UNIT 1)

PART OF CRYSTAL FILTER ASSEMBLY (M32-3461-01)

DIODE SWITCH

13

PLER D1 R1 R2 SKTL 6 PL — 100kc/s TEST SIGNAL TO PANEL FILTER SWITCHING UNIT 12

100kc/s I.F TEST (FROM MR17)

LSB A.F TO VT6 (FIG.14-3B)

DIODE SWITCH

C34 0·1 — MR10 CV7332 — R53 1k — C31 0·1 — R55 10k — R54 47k — C32 0·1 — R56 18k — -30V

R58 6·8k — C33 0·1 — R57 100k — R59 2·2k

R17 — 100kc/s I.F. TEST (TO PLF-5) — R94 220 — C53 ·047

+30V (Y) — R50 3·9k — R51 18k — C30 0·1 — R46 1·8k — R47 1·2k — C27 0·1 — C28 0·1 — VT5 A1505 — R52 12k — R48 150 — R49 2·2k — C29 0·1

R96 15k — MR20 CV7127 — C55 0·1

100kc/s LSB/SSB I.F. (FROM PLF-14)

R61 4·7k — MR11 MR12 — R62 100 — R63 100 — 4 x CV7127 — MR13 MR14 — R64 100 — R65 100 — R66 4·7k

C36 6·8 — R67 27k

T2 1 3 5 4 6

LSB DEMODULATOR

USB DEMODULATOR

R1 4·7k — MR1 R4 100 — R2 100 — 4 x CV7127 — MR2 MR3 — R3 100 — MR4 R5 100 — R6 4·7k

100kc/s USB/SSB I.F. (FROM PLF-16)

R7 27k — C1 6·8 — MR5 CV7332 — R9 39k — R10 100k — C2 6·8 — R8 1k — C3 6·8 — USB A.F. TO VT1 (FIG.14-3B) — R11 10k

+30V (Z) — R36 1·5k — R39 560 — C24 0·1 — T1 2 7 4 8 — C22 ·001 — C20 0·1 — R37 47k — C21 0·1 — VT4 A1505 — R38 6·8k — R40 220 — R41 820 — C23 0·1

DSB DETECTOR

MR8 CV7127 — R42 68k — R43 4·7k — RV2 5k — C25 6·8

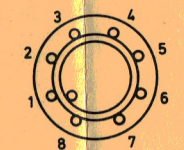
MR9 CV7332 — R44 39k — R45 100k — C26 6·8

MR19 CV7332 — R60 1k

AMPLIFIER

DIODE SWITCHES

BASE VIEWS



T1, T2 & L1, L2



ALL TRANSISTORS

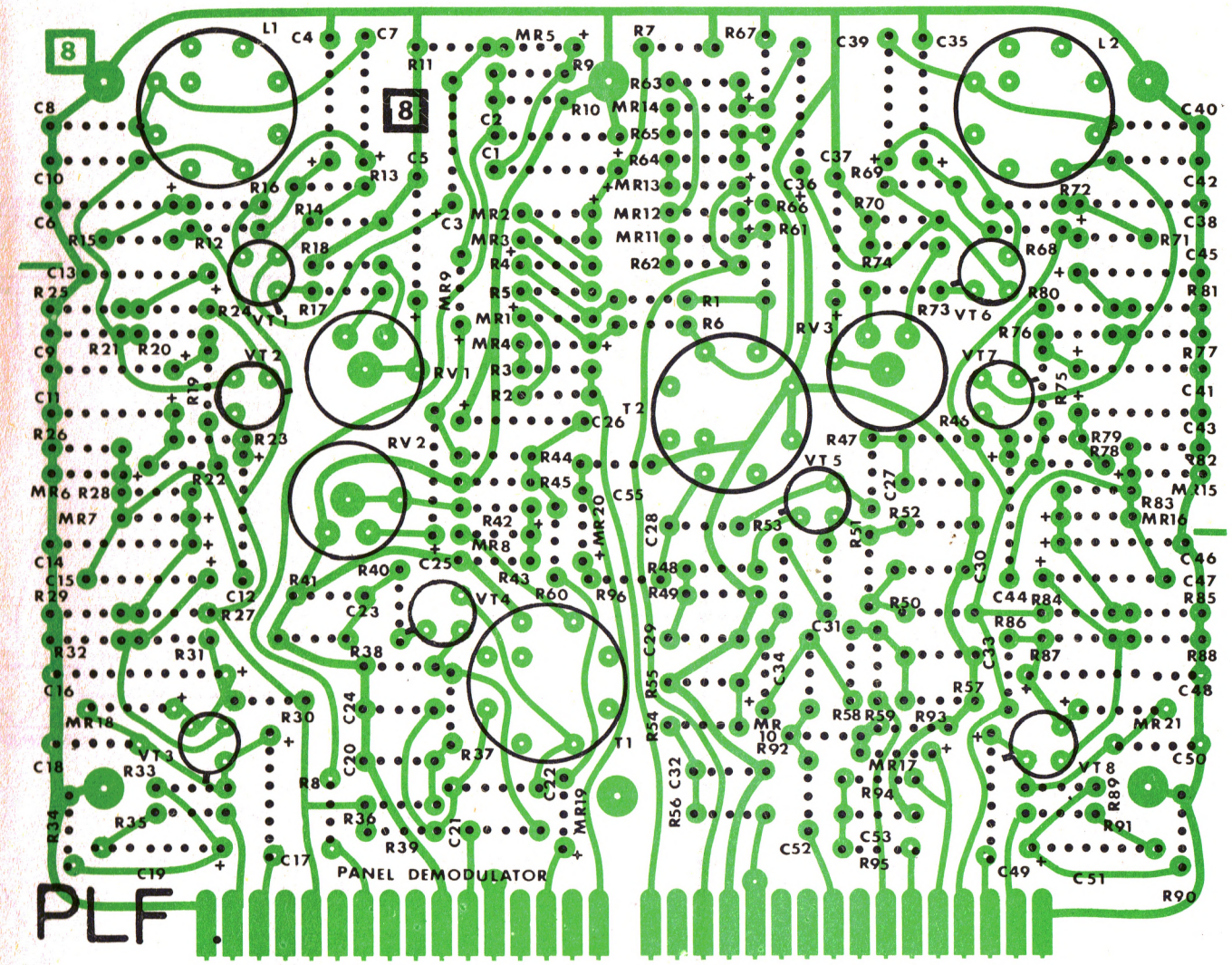
MOD RECORD

1	2	3	4	5	6
7	8	9	10	11	12

PANEL DEMODULATOR
SUB-ASSEMBLY 7

5820-99-519-7029
CIRCUIT DIAGRAM

FIG.14·3A



M32-2941 [L] ISS 8

FIG. 14.2 PANEL DEMODULATOR COMPONENT LAYOUT

B.R.4147 (5) A
Original

94 57 58 59 36 37 55 38 54 56 53 39 40 41 50 51 52 46 47 48 49 43 42 96 RV2 61 1 66 6 62 2 64 3 63 4 65 5 67 7 8 60 9 44 10 45 11 3 2 26 36 1 53 34 33 20 21 24 32 22 30 31 23 28 29 27 25 17 MR10 VT4 T1 VT5 MR8 T2 MR20 MR13 MR11 MR1 MR4 MR12 MR2 MR14 MR3 MR19 MR5 MR9

AMPLIFIER

METERING RECTIFIER

PLF 17 1SB2F-11 — METERING TO 1M1 (FREQ. CH. DRIVES -100kc/s)

5 (UNIT 1)

PART OF CRYSTAL FILTER ASSEMBLY (M32-3461-01)

DIODE SWITCH

13

PLER D1 R1 R2 SKTL 6 PL — 100kc/s TEST SIGNAL TO PANEL FILTER SWITCHING UNIT 12

100kc/s I.F TEST (FROM MR17)

LSB A.F TO VT6 (FIG.14-3B)

DIODE SWITCH

C34 0·1 — MR10 CV7332 — R53 1k — C31 0·1 — R55 10k — R54 47k — C32 0·1 — R56 18k — -30V

R58 6·8k — C33 0·1 — R57 100k — R59 2·2k

R17 — 100kc/s I.F. TEST (TO PLF-5) — R94 220 — C53 ·047

+30V (Y) — R50 3·9k — R51 18k — C30 0·1 — R46 1·8k — R47 1·2k — C27 0·1 — C28 0·1 — VT5 A1505 — R52 12k — R48 150 — R49 2·2k — C29 0·1

R96 15k — MR20 CV7127 — C55 0·1

100kc/s LSB/SSB I.F. (FROM PLF-14)

R61 4·7k — MR11 MR12 — R62 100 — R63 100 — 4 x CV7127 — MR13 MR14 — R64 100 — R65 100 — R66 4·7k

C36 6·8 — R67 27k

T2 1 3 5 4 6

LSB DEMODULATOR

USB DEMODULATOR

R1 4·7k — MR1 R4 100 — R2 100 — 4 x CV7127 — MR2 MR3 — R3 100 — MR4 R5 100 — R6 4·7k

100kc/s USB/SSB I.F. (FROM PLF-16)

R7 27k — C1 6·8 — MR5 CV7332 — R9 39k — R10 100k — C2 6·8 — R8 1k — C3 6·8 — USB A.F. TO VT1 (FIG.14-3B) — R11 10k

+30V (Z) — R36 1·5k — R39 560 — C24 0·1 — T1 2 7 4 8 — C22 ·001 — C20 0·1 — R37 47k — C21 0·1 — VT4 A1505 — R38 6·8k — R40 220 — R41 820 — C23 0·1

DSB DETECTOR

MR8 CV7127 — R42 68k — R43 4·7k — RV2 5k — C25 6·8

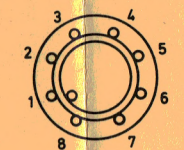
MR9 CV7332 — R44 39k — R45 100k — C26 6·8

MR19 CV7332 — R60 1k

AMPLIFIER

DIODE SWITCHES

BASE VIEWS



T1, T2 & L1, L2



ALL TRANSISTORS

MOD RECORD

1	2	3	4	5	6
7	8	9	10	11	12

PANEL DEMODULATOR
SUB-ASSEMBLY 7

5820-99-519-7029
CIRCUIT DIAGRAM

FIG.14·3A

| | | |

| | | |

CHAPTER 14A

PANEL DEMODULATOR 5820-99-758-9179

UNIT 7A

CONTENTS

Paragraphs

1 Introduction
5 Physical Description
7 Electrical Description
13 For Link 11 use

ILLUSTRATIONS

Figure

14A.1 Panel Demodulator Block Diagram
14A.2 Panel Demodulator Component Layout
14A.3A Panel Demodulator Circuit Diagram
14A.3B Panel Demodulator Circuit Diagram
14A.3C Panel Demodulator Circuit Diagram

CHAPTER 14A

PANEL DEMODULATOR 5820-99-758-9179

UNIT 7A

Introduction

Figure 14A.1

1 IF inputs from Units 10 and 11 are demodulated in the Panel Demodulator to provide af outputs for Amplifier Audio Frequency, unit 5. Separate but similar circuits for usb and lsb signals each comprise a detector and a two stage af amplifier which provides low-pass filtering and an emitter-follower output.

2 Demodulation is effected by an envelope detector for dsb reception and by balanced modulators for ssb reception. The re-insertion carrier frequency of 100 kHz for the balanced modulators is obtained from the Synthesizer. The dsb or ssb input to the upper sideband af amplifier is switched by MR5, MR9 which may be considered as a single pole change-over switch controlled by RECEIVE USB/DSB switching on the front panel.

3 On dsb and mcw, MR9 is closed and MR5 open. On all other modes MR9 is open and MR5 closed. MR10 operates at the same time as MR5 to switch the 100 kHz carrier to the ssb demodulators.

4 A 100 kHz test signal is switched to Unit 13 via PLF5 by MR17 when the METERING switch on the front panel is set to IF TEST ON DSB - 100 kHz.

Physical Description

5 Unit 7A is a plug-in printed wiring board 7.2 inches by 5.5 inches. A finger pull facilitates removal and slotted guides assist location into its socket. Rubber pads on the printed wiring side prevent it being mounted in the wrong position. The screen on each side is earthed by its mounting pillars.

6 Three preset potentiometers, adjusted during initial setting-up, are mounted on the panel. They are accessible through holes in the front screen.

Electrical Description

Figure 14A.3A, 3B & 3C

7 The usb and lsb channels are similar in action, but diode switching enables a dsb signal to be routed through the usb channel when required. Only the usb channel is described.

8 The if signal from Amplifier Intermediate Frequency (100 kHz), unit 10 appears at PLF16 and is applied across the balanced modulator MR1-4, R2-5. The 100 kHz input from the Synthesizer at PLF9 is passed via MR10 switching circuit to amplifier VT5 which supplies T2. The centre tapped secondary of T2 provides the re-insertion input to the balanced modulator via R1, R6.

9 The resultant output, at audio frequency, is amplified by VT1, for low-pass filtering in the sideband filter L1, C8, C10 and further amplified by VT2. VT3 is an emitter-follower which provides af outputs for the Amplifier Audio Frequency, unit 5(5A) and for monitoring.

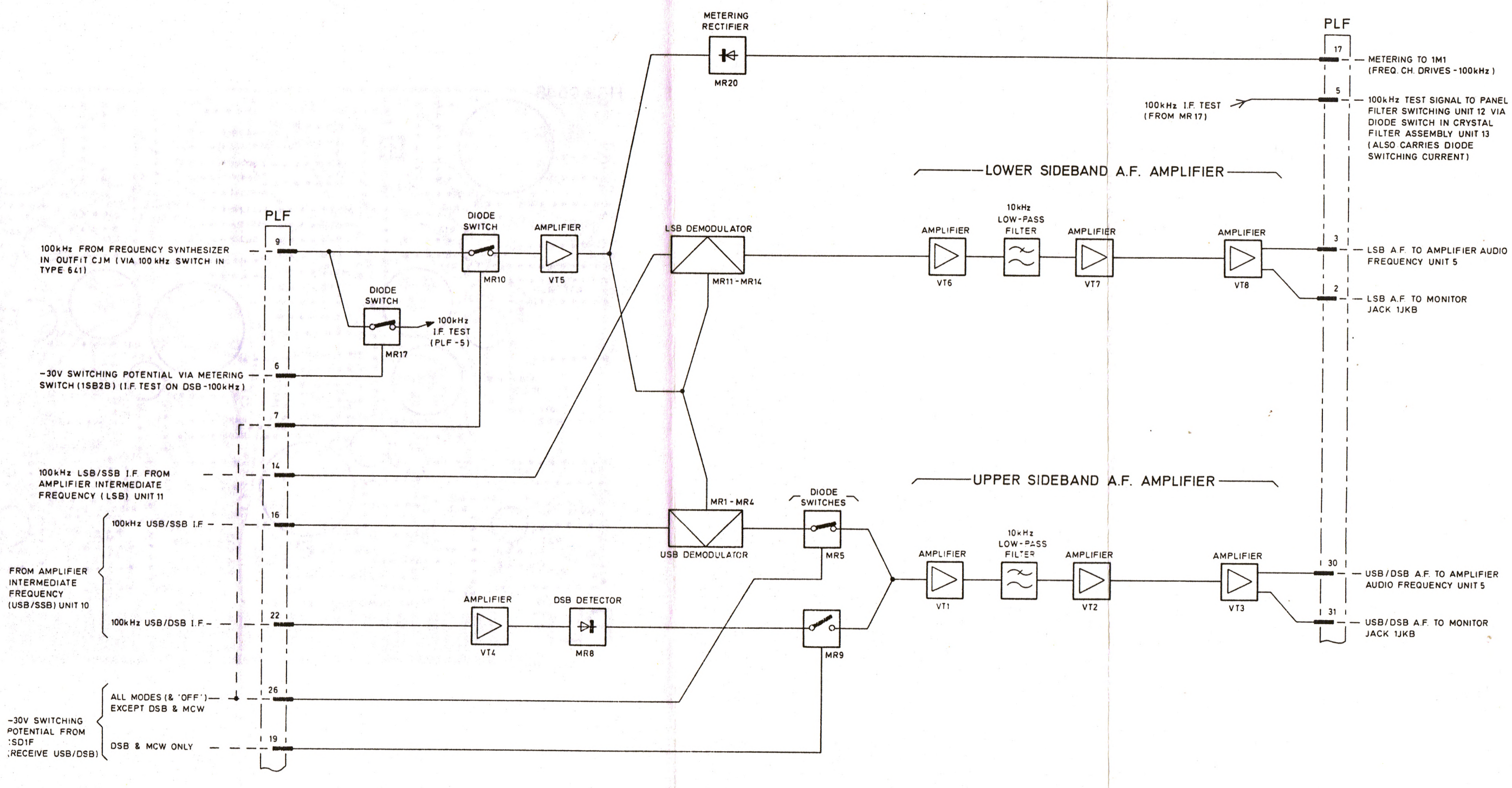
10 During ssb, cw, fst and DATA operation, -30 V is applied to PLF26 and PLF7. This allows diodes MR5 and MR10 to conduct. MR10 allows the 100 kHz carrier from the Frequency Synthesizer to pass, via amplifier VT5, to the ssb detector. MR5 allows the demodulated signal output from the ssb detector to pass to VT1. Under this condition there is no -30 V on PLF19, and MR9 is non-conducting.

11 During dsb or mcw operation, the -30 V is removed from PLF26 and PLF27, thus applying reverse bias to MR5 and MR10 via R10 and R57 respectively, so that these both present a high degree of attenuation to the signals. Under these conditions -30 V is applied to PLF19, so causing MR9 to conduct and present a low-impedance path to the signal from the dsb detector to VT1 base.

12 MR18, MR21 protect VT3, VT8 from accidental damage without affecting their normal operation. For example, if unit 7A is unplugged without switching off the equipment and allowing a short time for capacitors to discharge, C17 and C49 will be charged to 20V and will retain this charge. If unit 7A is then plugged into a receiver which may be switched on or off, it is possible to discharge these capacitors via PLP3 or PLP30, via the emitter/base junction of VT3 and VT8 respectively. This could damage the relevant transistor if MR18 and MR21 did not provide protection.

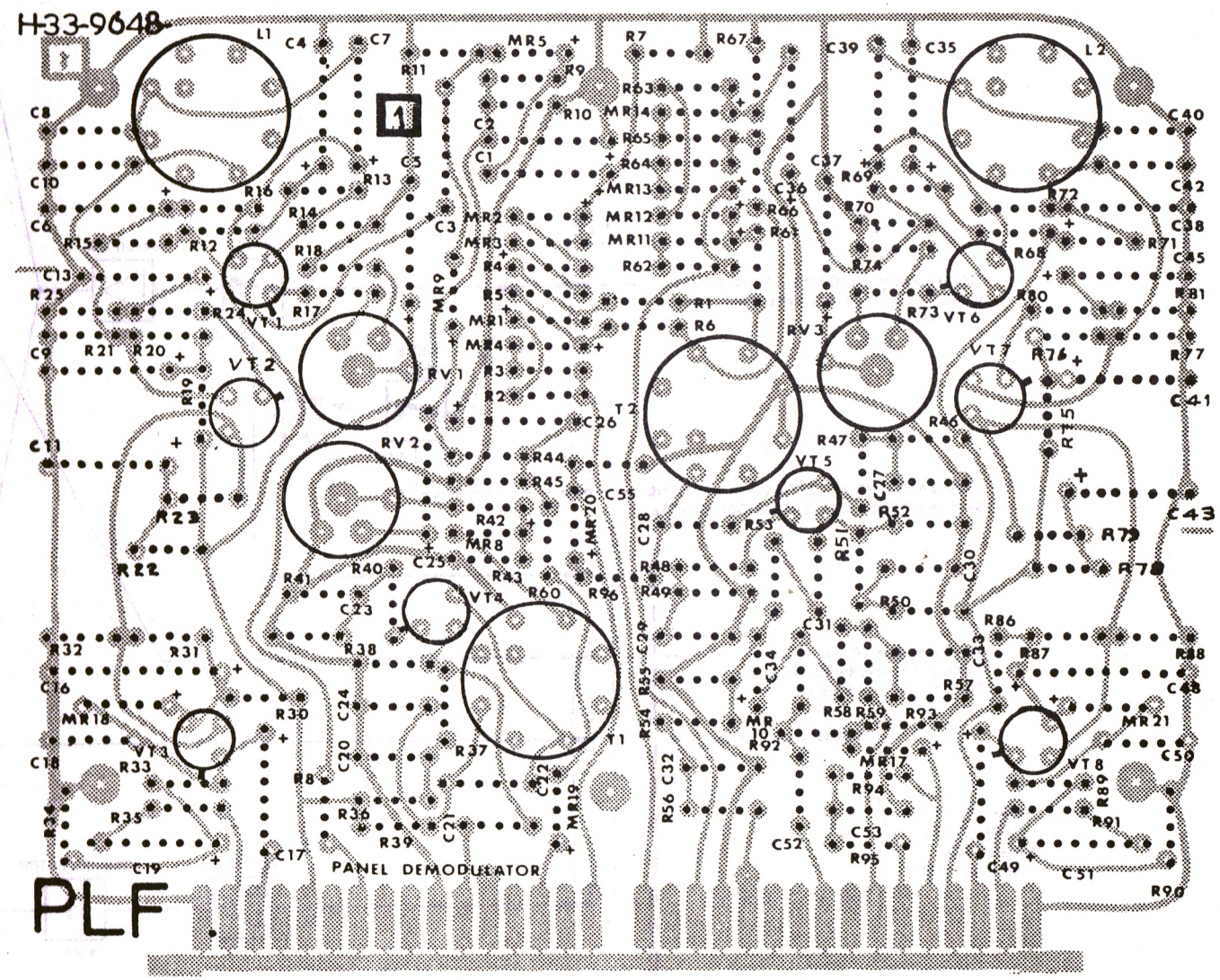
For Link 11 use

13 Panel Demodulator 5820-99-758-9179 must be used together with Panel Automatic Gain Control 5820-99-758-9181 and Board Amplifier Audio Frequency 5820-99-758-9180. Panel Modulator 5820-99-758-9179 may be used in a normal CJM installation with Panel Automatic Gain Control 5820-99-519-7028 and/or Amplifier Audio Frequency 5820-99-519-7030.



PANEL DEMODULATOR 5820-99-758-9179
SUB-ASSEMBLY 7A BLOCK DIAGRAM

FIG. 14A.1

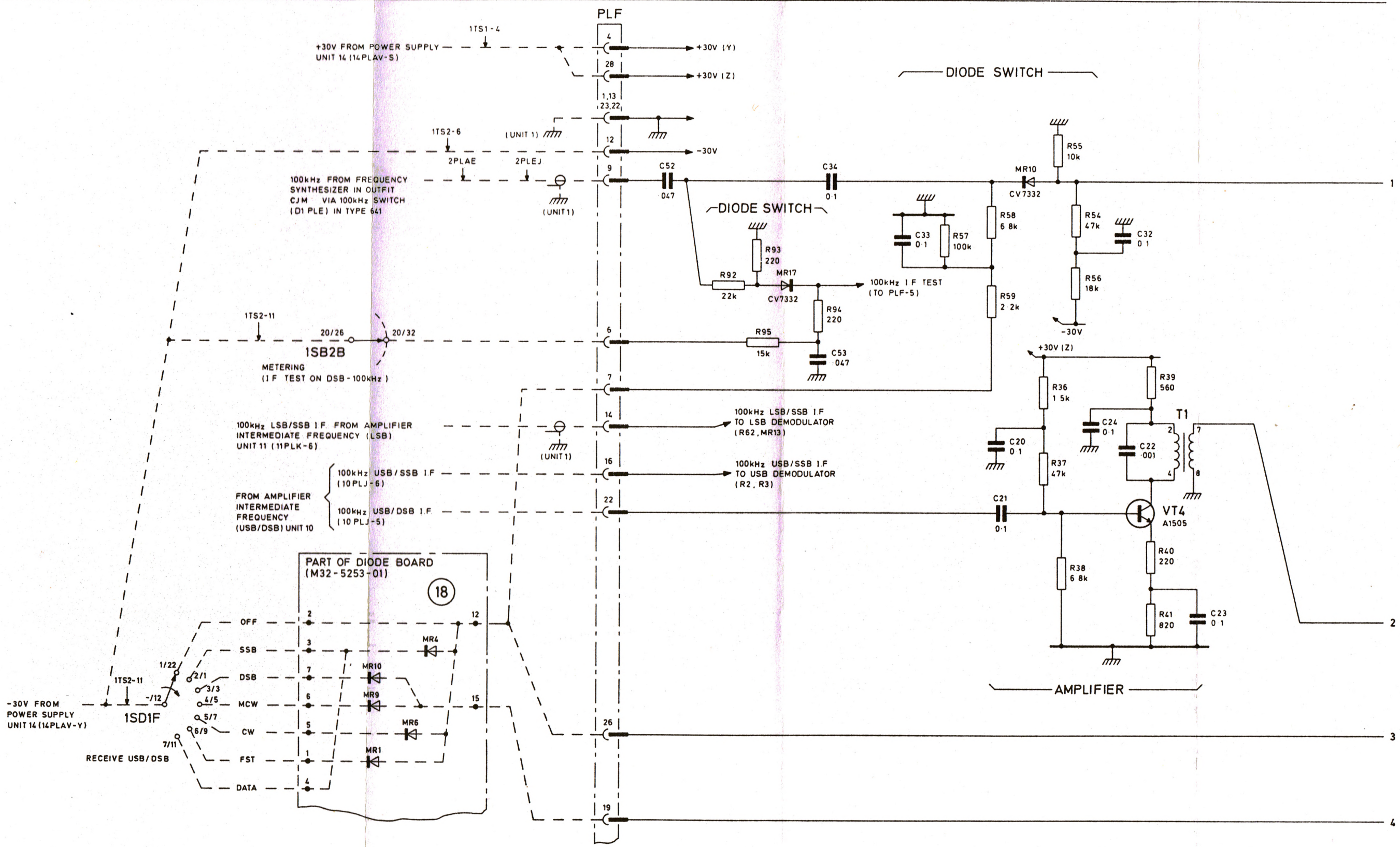


PANEL DEMODULATOR
COMPONENT LAYOUT

FIG 14A.2

B.R. 4147 (5)A
Ambt. 7, 12,84

RES.	92 93 95 94 57 58 59 36 37 55 38 54 56 39 40 41
CAP	52 53 34 33 20 21 24 32 22 23
MISC	MR17 MR10 VT4 T1



PANEL DEMODULATOR 5820-99-758-9179
SUB-ASSEMBLY 7A CIRCUIT DIAGRAM

FIG 14A. 3A

| | | |

| | | |

CHAPTER 15

AMPLIFIER AUDIO FREQUENCY 5820-99-519-7030

UNIT 5

CONTENTS LIST

	Paragraphs
Introduction	1 - 6
Physical Description	7
ELECTRICAL DESCRIPTION	8 - 22
Diode Switches	8 - 12
Line Amplifiers	13 - 25
Line Monitoring	16 - 18
Loudspeaker Amplifier	19 - 22

ILLUSTRATIONS

	Figure No
Simplified Diode Switch Operation	15.1
Amplifier Audio Frequency Block Diagram	15.2
Amplifier Audio Frequency Component Layout	15.3
Amplifier Audio Frequency Circuit Diagram	15.4 A, B

CHAPTER 15

AMPLIFIER AUDIO FREQUENCY 5820-99-519-7030

UNIT 5

Introduction

Figure 15.2

1. The Amplifier Audio Frequency contains three line amplifiers and a loudspeaker amplifier. Signal routing is achieved by diode switches which are energised by switches on the Receiver front panel.

2. There are two independent audio inputs from Panel Demodulator Unit 7, one from the usb and one from the lsb channel. Either input may be routed to any one of the line amplifiers, giving a balanced output to one local and two remote operator positions. Also either input may be routed via a volume control to a loudspeaker amplifier and then to the loudspeaker on the front panel. The signal on any line amplifier may be monitored by a headset plugged in to the H/SET socket on the front panel. The monitoring amplifier is part of the Panel Receiver Auxiliary Circuits, unit 6.

3. The A.G.C. of the Receiver holds each channel output, usb or lsb, to the same P.E.P. irrespective of the received signal level which is from 1 μV to 1 V. The audio inputs at PLE6, 7 are therefore at a constant level of approximately 2.3 V.

4. The line amplifiers have fixed gain and provide the required line output level at low distortion. The nominal output level is 4.0 V on open circuit with an output impedance of 200 ohms which is capable of being connected in parallel with the sidetone output of an associated auto-tuning transmitter with similar characteristics. Any level setting required is done at the line terminal equipment. Since it is possible to switch both input channels to one line output, the two input circuits are arranged to load each other to drop each input level by 6 dB and prevent overloading and distortion in the amplifier.

5. During reception of dsb signals the usb channel is employed and preceding circuitry set so that P.E.P. ssb and 90% modulated dsb give the same audio output. The loudspeaker amplifier has an output capability of 1 W and sufficient gain to give this output for a 30% modulated dsb signal. The gain of this amplifier and that of the monitor amplifier is controlled by the VOLUME control on the front panel.

6. The headset circuit monitors the signal on the line to which it is connected, whether the signal is produced by the Receiver or applied to the line by an external source. Connection of a transmitter drive sidetone output to the line allows both transmitted and received signals to be monitored.

Physical Description

7. Unit 5 is a plug-in printed-wiring board 7.2 inches by 5.5 inches. A finger pull facilitates removal and slotted guides assist location of the board into its socket. Rubber pads on the printed-wiring side prevent it from being inserted in the wrong position.

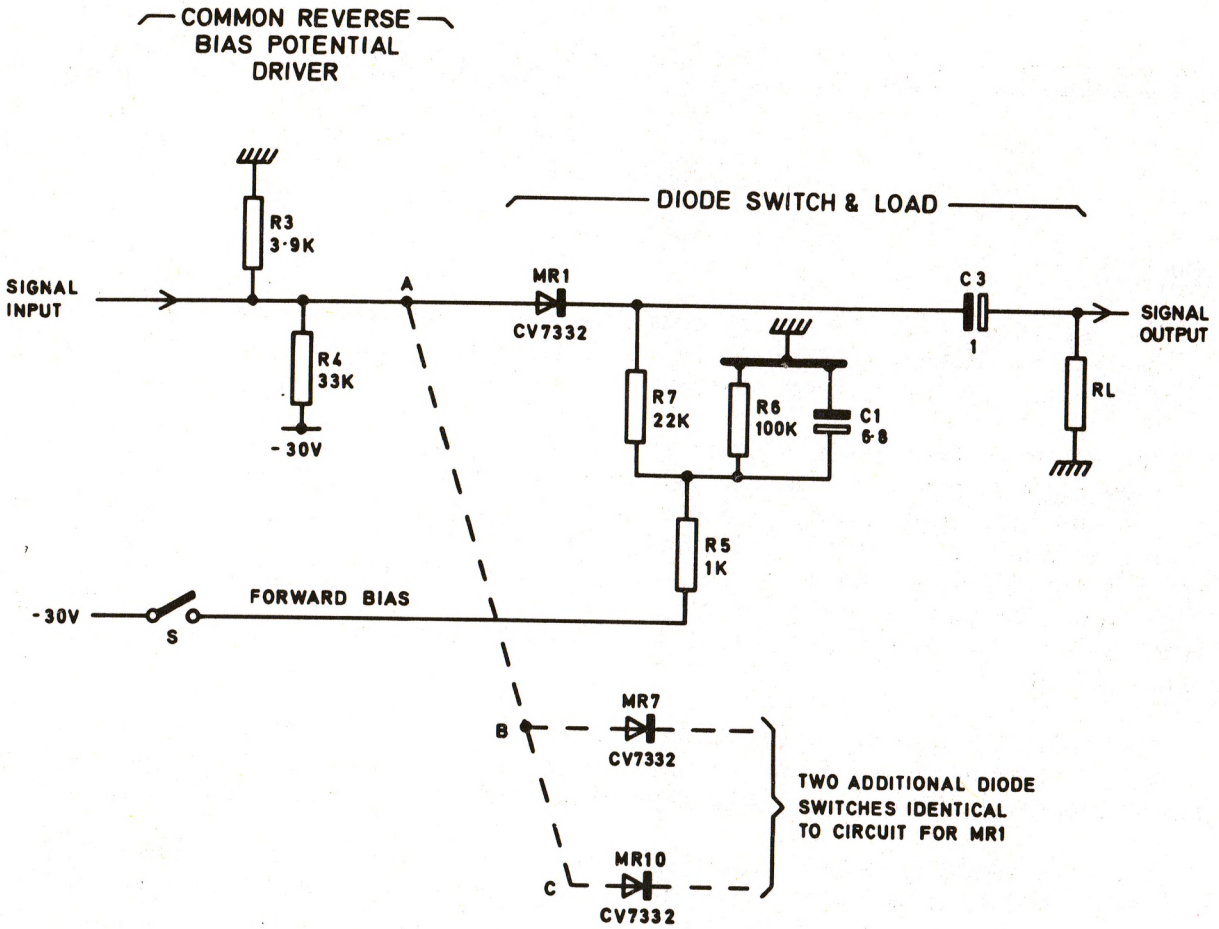


Fig 15.1 SIMPLIFIED DIODE SWITCH OPERATION

Diode Switches

Figures 15.1, 15.4

8. The diode switches are identical in operation and one circuit is described in detail.

9. MR1 is back-biased by approximately 3.1 V provided by the fixed potentiometer network R3, R4 across the -30 V supply. The diode return path is via R6, R7 to earth. In this state the circuit will stand an input signal of approximately 3.1 V peak without breakthrough.

10. To forward bias the diode and thus produce a low-impedance transmission path to RL, -30 V is applied via switch S, R5, R7 to the cathode of the diode. R5, R7, R3 and the difference in potential between 3.2 V and 30 V are the main factors controlling the diode forward current. This current is approximately twice the peak signal current to be handled, to give low forward loss and low distortion.

11. R7, C1 decouple the switching line from any high a.c. voltage. If the 30 V supply presents a lower impedance than C1, the switching line is safeguarded against a.c. current by R5.

12. If three outputs are required from the same source, the back-biasing network is made common to three identical switching circuits at A, B and C.

Line Amplifiers — Figure 15.4A

13. The amplifiers for operator positions LOC, REM1 and REM2 are identical. The LOC line amplifier VT1, VT2, VT3 is described. VT1 is a common emitter amplifier with negative feedback, d.c. coupled to emitter-followers VT2 and VT3.

14. The input is applied to the junction R12, R13 which determines VT1 base bias. The gain is precisely set by the ratio between the load R14 and emitter feedback resistor R15. The output impedance is determined by R19 and the winding resistance of T1. R out is approximately 220 ohms. C7, C8 prevent high-frequency oscillation.

15. The usb input to the amplifier is via attenuator network R1, R2, R3 and diode switch MR1. The attenuator network reduces the audio level from the demodulator to a more convenient level for the line amplifier diode switches. This causes the gain per channel to drop by approximately 6 dB when both usb and lsb channels are switched to the same line amplifier.

Line Monitoring — Figure 15.4A

16. Any one of the three line amplifier outputs may be switched to the monitor output at PLE21. On the LOC line output the diode switch comprises C10, R20, R21, C11, R22 and MR3 with biasing network R64, R63, which is common to all three switches. The REM1 and REM2 circuits are identical in action to the LOC monitor circuit, MR9 and MR12 being the diode switches.

17. Diode switches MR3, MR9, MR12 are controlled by the right hand, headset, MONITORING switch 1SJ and by the LOC-REM1-REM2 line selector switch 1SC or 1SE on the RECEIVE USB/DSB or the RECEIVE LSB panel. For instance, with 1SJ on USB/DSB and 1SC to REM1, -30 V is routed to R62 to forward bias MR9 so that the REMOTE 1 line amplifier output is monitored. At the same time the LSB line selector 1SE would normally be set to the other remote position REM2 so that on switching 1SJ to LSB, the REMOTE 2 line amplifier output is monitored.

18. If both line selector switches are set to the same position, say to LOC, then the local line amplifier output can be monitored with the headset MONITORING switch 1SJ at USB/DSB or LSB although the signal may be available on only one channel.

Loudspeaker Amplifier — Figure 15.4B

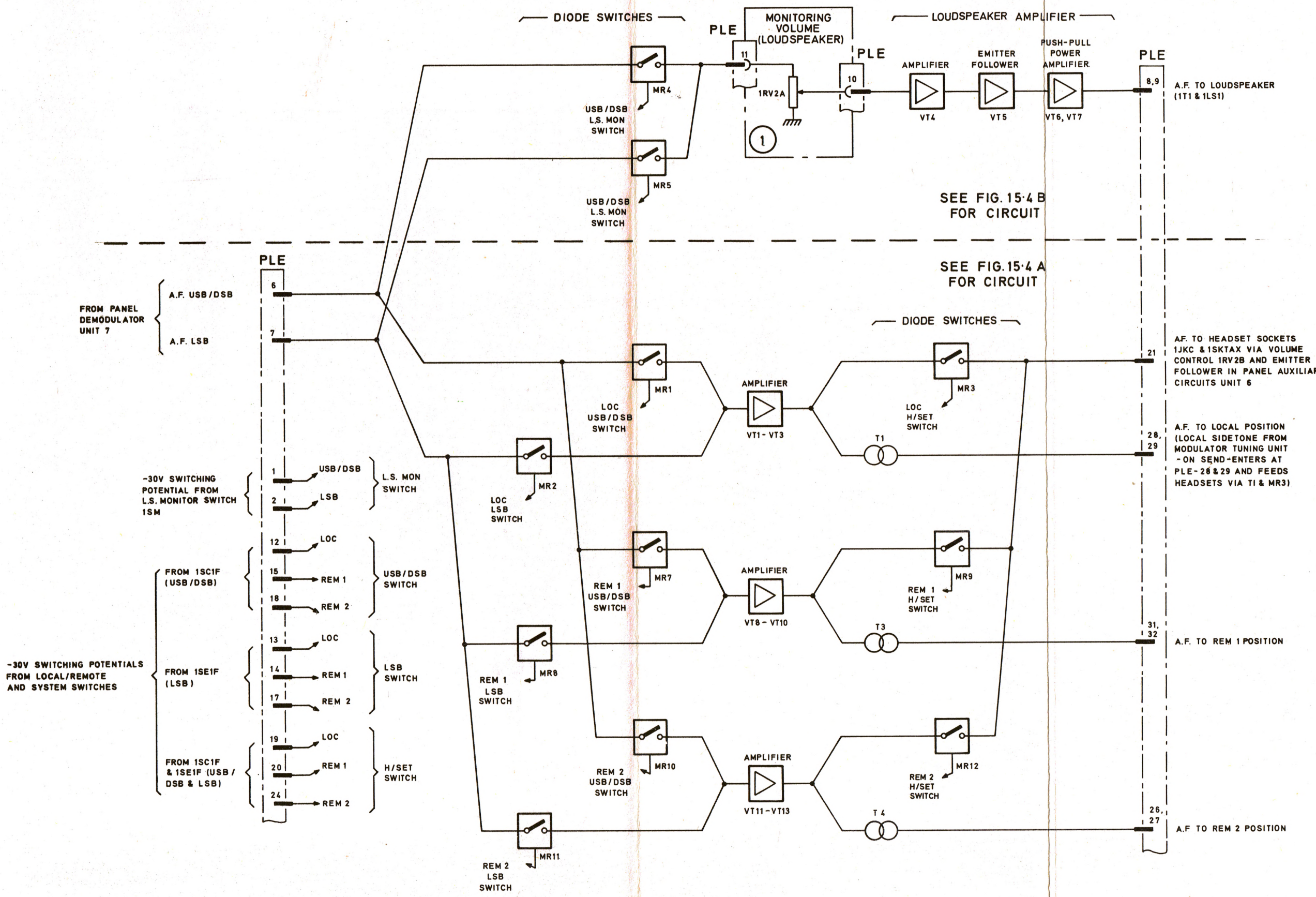
19. The usb or lsb channel input is applied to the loudspeaker amplifier by diode switches MR4 and MR5, via VOLUME control 1RV2A.

20. The amplifier comprises VT4, VT5, VT6 and VT7. The input is fed to the junction R31, R32, the base bias resistors of VT4. R33 limits the drop in input impedance should the amplifier be overdriven. VT4 is a common emitter stage with feedback, gain being precisely controlled by R35 and R36. VT4 is d.c. coupled to emitter-follower VT5 which is transformer coupled to the Class B push-pull pair VT6, VT7. C20 inhibits any tendency to high frequency oscillation.

21. VT5 prevents the relatively low input impedance of VT6, VT7 loading VT4 unduly, and provides a low source impedance to the output pair, making it unnecessary to match them.

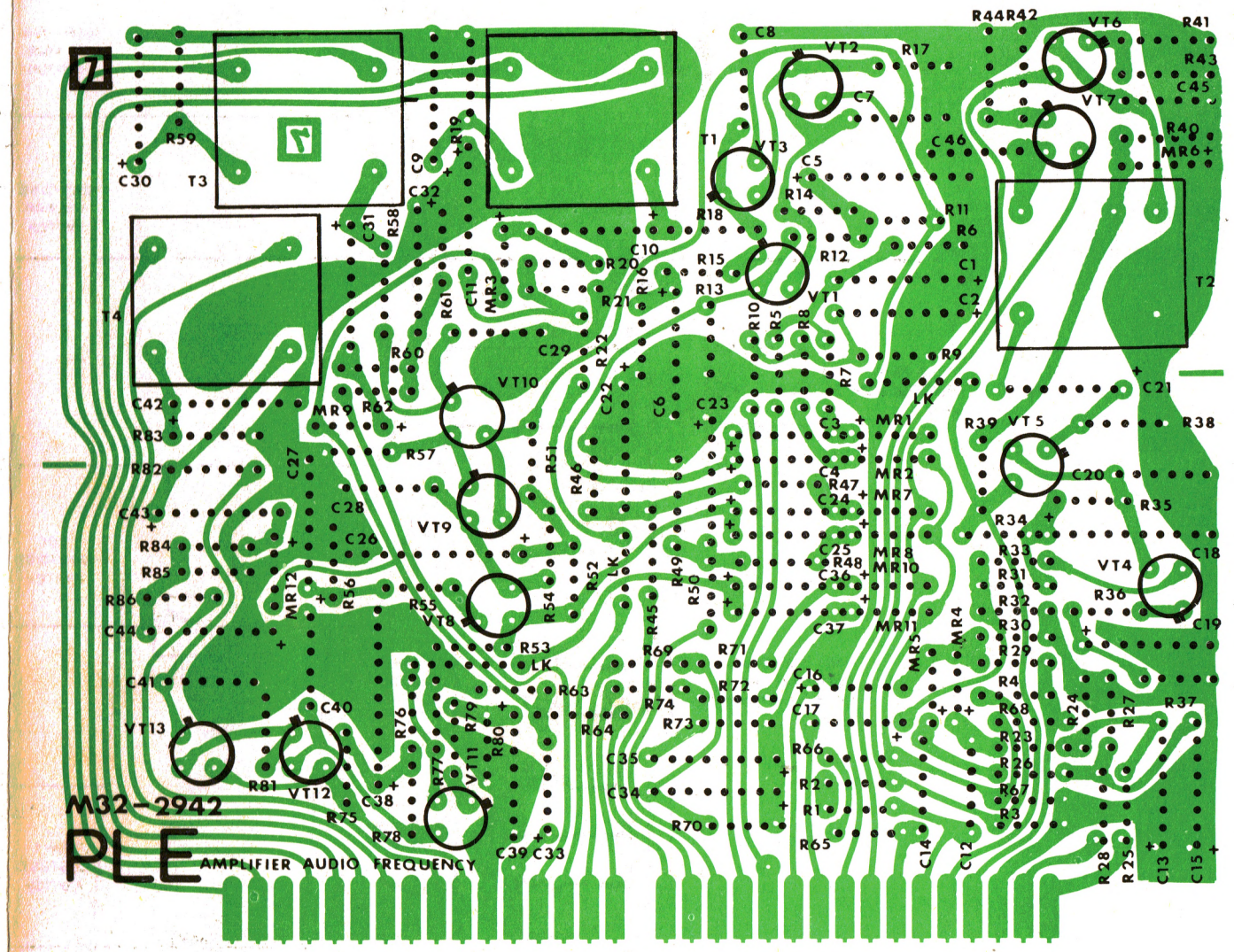
22. T2 has a 1:1:1 ratio, the centre tapped secondary providing phase opposing drives to VT6 and VT7. The network R39, R40 and MR6 across the +30 V supply applies a small bias, via T2, to VT6 and VT7 which reduces cross-over distortion. MR6 varies the bias voltage with temperature and compensates for the changing requirements of the transistors.

| | | |



AMPLIFIER AUDIO FREQUENCY 5820-99-519-7030
SUB ASSEMBLY 5 BLOCK DIAGRAM

FIG 15·2



M32-2942 [L] ISS 7

15.3 AMPLIFIER AUDIO FREQUENCY COMPONENT LAYOUT

PLE

DIODE SWITCHES

A.F FROM PANEL DEMODULATOR UNIT 7

FROM POWER SUPPLY UNIT 1

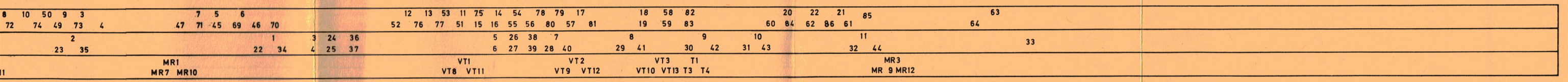
-30V FROM POWER SUPPLY UNIT 14 (14 PLAY-Y)

RECEIVE USB/DSB

RECEIVE LSB

PART OF DIODE BOARD (M32-5253-01)

	RES	CAP	MISC
	1 2 65 66 67 68 8 10 50 9 3 72 48 74 73 4 7 5 6 69 46 70 47 71 45 4 12 13 53 11 75 14 54 52 76 77 51 15 16 55	2 23 35 1 22 34 4 25 37 3 24 36 5 26 6 27	MR2 MR8 MR11 MR1 MR7 MR10 VT1 VT8 VT11



DIODE SWITCHES

(W) R3 3·9k — R4 33k — -30V (Y)

MR1 CV7332 — R7 22k — R6 100k — C1 6·8 — R5 1k — LOC USB / DSB SWITCH (PLE -12) — C3 1

(W) R8 22k — R9 100k — C2 6·8 — R10 1k — LOC LSB SWITCH (PLE -13) — C4 1

MR7 CV7332 — (W) R47 22k — R46 100k — C22 6·8 — R45 1k — H — REM-1 USB/DSB SWITCH (PLE -15) — C24 1

(W) R48 22k — R49 100k — C23 6·8 — R50 1k — REM 1 LSB SWITCH (PLE -14) — C25 1

MR10 CV7332 — (W) R71 22k — R70 100k — C34 6·8 — R69 1k — REM 2 USB/DSB SWITCH (PLE -16) — C36 1

(W) R72 22k — R73 100k — C35 6·8 — R74 1k — REM 2 LSB SWITCH (PLE-17) — C37 1

LOCAL LINE AMPLIFIER

+30V (U) — R11 820

R12 82k — R14 5·6k — C5 22 (W)

VT1 A1505 — C7 680p (W) — VT2 A1505 — VT3 2N1613

R13 12k — R15 470 — R16 680 — C6 15 (W)

R17 1·8k (W) — C8 ·0015 (W) — R18 120

T1 — 28 TO PLE 29 — LOC O/P

R19 270 — C9 15 (X)

C10 6·8

REMOTE 1 LINE AMPLIFIER
(SEE LOCAL AMPLIFIER ABOVE & NOTE 2)

R51 — R52 — R54 — C26 (X) — C28 (X)

VT8 — VT9 — VT10

R53 — R55 — R56 — C27 (X) — R57 (X) — C29 (X) — R58

T3 — 31 TO PLE 32 — REM 1 O/P

R59 — C30 (X)

REMOTE 2 LINE AMPLIFIER
SEE LOCAL AMPLIFIER ABOVE & NOTE 2

R75 — R76 — R78 — C38 (X) — C40 (X)

VT11 — VT12 — VT13

R77 — R79 — R80 — C39 (X) — R81 (X) — C41 (X) — R82

T4 — 26 TO PLE 27 — REM2 O/P

R83 — C42 (X)

DIODE SWITCHES

C10 6·8 — MR3 CV7332 — (X) R20 6·8k — R21 100k — C11 6·8 — R22 470 — LOC H/SET SWITCH (PLE-19)

(W) R63 10k — R64 22k — -30V (Z) — C33 1

C31 6·8 — MR9 CV7332 — (X) R60 6·8k — R61 100k — C32 6·8 — R62 470 — REM 1 H/SET SWITCH (PLE-20)

C43 6·8 — MR12 CV7332 — (X) R84 6·8k — R85 100k — C44 6·8 — R86 470 — REM 2 H/SET SWITCH (PLE-24)

NOTES
1 LOCAL SIDETONE FROM MODULATOR TUNING UNIT (ON SEND) ENTERS AT 1 PLAA-HH & EE AND IS FED TO HEADSET VOLUME CONTROL 1RV2B VIA T1, MR3 & PLEE -21

2 EXCEPT FOR POWER RAILS THE CIRCUITS OF ALL THREE LINE AMPLIFIERS ARE IDENTICAL COMPONENT VALUES FOR REMOTE LINE AMPLIFIERS MAY BE OBTAINED BY REFERENCE TO THE LOCAL AMPLIFIER CIRCUIT WHICH IS DRAWN IN FULL

PLE

21 — MONITORING VOLUME (H/SET) — GANGED TO 1RV1A (FIG 15-4B) — 1RV2B — A.F. TO EMITTER FOLLOWER IN PANEL AUXILIARY CIRCUITS UNIT 6 (6 PLC -3) — (UNIT 1)

LOC O/P FROM T1 — 28 — 1 PLAA HH — 29 — EE — A.F. TO LOCAL POSITION (SEE NOTE 1) — (UNIT 1)

REM 1 O/P FROM T3 — 31 — 1 PLAA AA — 32 — CC — A.F. TO REM 1 POSITION — (UNIT 1)

REM 2 O/P FROM T4 — 26 — 1 PLAA W — 27 — Y — A.F. TO REM 2 POSITION — (UNIT 1)

MOD RECORD					
1	2	3	4	5	6
7	8	9	10	11	12

AMPLIFIER AUDIO FREQUENCY 5820-99-519-7030
SUB-ASSEMBLY 5 — CIRCUIT DIAGRAM

FIG. 15-4A

CHAPTER 15A

AMPLIFIER AUDIO FREQUENCY

5820-99-758-9180

UNIT 5A

CONTENTS

Paragraphs

1 Introduction
7 Physical Description
ELECTRICAL DESCRIPTION
8 Diode Switches
13 Line Amplifiers
Line Monitoring
19 Loudspeaker Amplifier
23 For Link 11 use

ILLUSTRATIONS

Figure

15A.1 Simplified Diode Switch Operation
15A.2 Amplifier Audio Frequency Block Diagram
15A.3 Amplifier Audio Frequency Component Layout
15A.4A Amplifier Audio Frequency Circuit Diagram
15A.4B Amplifier Audio Frequency Circuit Diagram
15A.4C Amplifier Audio Frequency Circuit Diagram

CHAPTER 15A

AMPLIFIER AUDIO FREQUENCY

5820-99-758-9180

UNIT 5A

Introduction

Figure 15A.1

1 The Amplifier Audio Frequency contains three line amplifiers and a loudspeaker amplifier. Signal routing is achieved by diode switches which are energized by switches on the Receiver front panel.

2 There are two independent audio inputs from Panel Demodulator Unit 7(7A), one from the usb and one from the lsb channel. Either input may be routed to any one of the line amplifiers, giving a balanced output to one local and two remote operator positions. Also either input may be routed via a volume control to a loudspeaker amplifier and then to the loudspeaker on the front panel. The signal on any line amplifier may be monitored by a headset plugged in to the H/SET socket on the front panel. The monitoring amplifier is part of the Panel Receiver Auxiliary Circuits, unit 6.

3 The AGC of the Receiver holds each channel output, usb or lsb, to the same PEP irrespective of the received signal level which is from 1 μV to 1 V. The audio inputs at PLE6, 7 are therefore at a constant level of approximately 2.3 V.

4. The line amplifiers have fixed gain and provide the required line output level at low distortion. The nominal output level is 4.0 V on open circuit with an output impedance of 200Ω which is capable of being connected in parallel with the sidetone output of an associated auto-tuning transmitter with similar characteristics. Any level setting required is done at the line terminal equipment. Since it is possible to switch both input channels to one line output, the two input circuits are arranged to load each other to drop each input level by 6 dB and prevent overloading and distortion in the amplifier.

5 During reception of dsb signals the usb channel is employed and preceding circuitry set so that PEP ssb and 90% modulated dsb give the same audio output. The loudspeaker amplifier has an output capability of 1W and sufficient gain to give this output for a 30% modulated dsb signal. The gain of this amplifier and that of the monitor amplifier is controlled by the VOLUME control on the front panel.

6 The headset circuit monitors the signal on the line to which it is connected, whether the signal is produced by the Receiver or applied to the line by an external source. Connection of a transmitter drive sidetone output to the line allows both transmitted and received signals to be monitored.

Physical Description

7 Unit 5A is a plug-in printed-wiring board 7.2 inches by 5.5 inches. A finger pull facilitates removal and slotted guides assist location of the board into its socket. Rubber pads on the printed-wiring side prevent it from being inserted in the wrong position.

ELECTRICAL DESCRIPTION

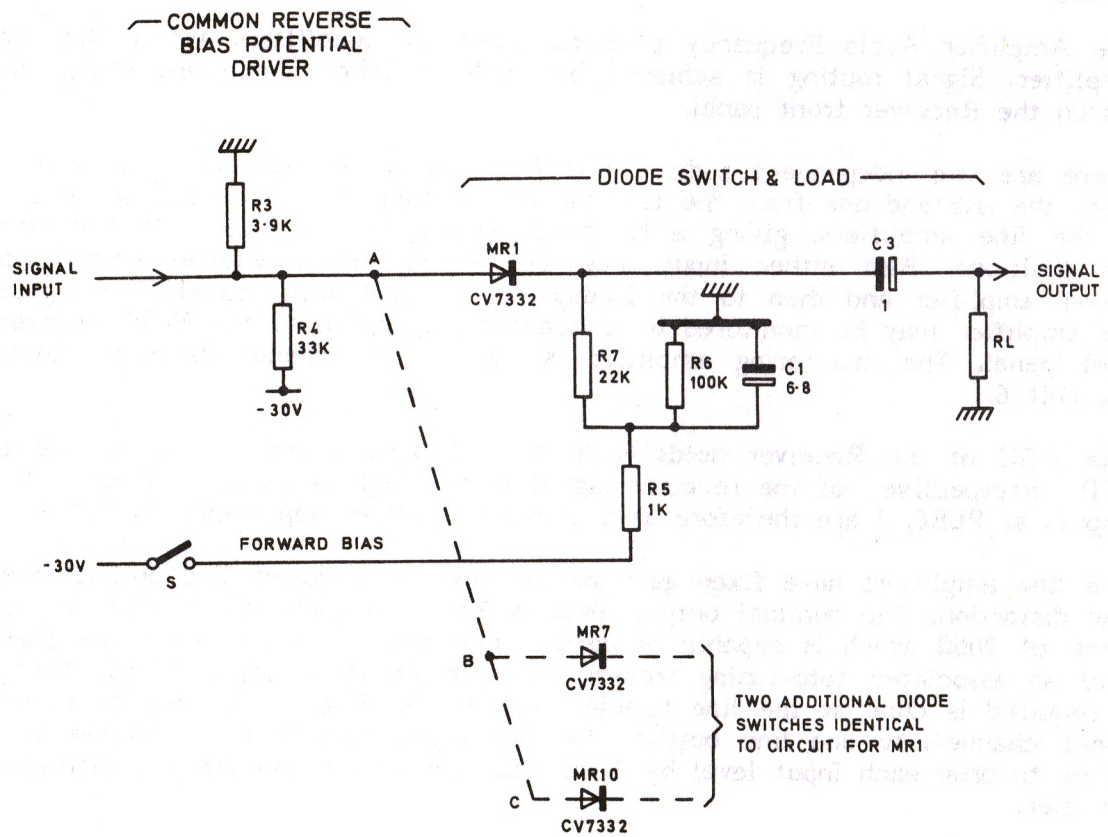


FIG.15A.1 SIMPLIFIED DIODE SWITCH OPERATION

Diode Switches — Figures 15A.1, 15A.4.A

8 The diode switches are identical in operation and one circuit is described in detail.

9 MR1 is back-biased by approximately 3.1 V provided by the fixed potentiometer network R3, R4 across the -30 V supply. The diode return path is via R6, R7 to earth. In this state the circuit will stand an input signal of approximately 3.1 V peak without breakthrough.

10 To forward bias the diode and thus produce a low-impedance transmission path to RL, -30 V is applied via switch S, R5, R7 to the cathode of the diode. R5, R7, R3 and the difference in potential between 3.2 V and 30V are the main factors controlling the diode forward current. This current is approximately twice the peak signal current to be handled, to give low forward loss and low distortion.

11 R7, C1 decouple the switching line from any high a.c. voltage. If the 30 V supply presents a lower impedance than C1, the switching line is safeguarded against a.c. current by R5.

12 If three outputs are required from the same source, the back-biasing network is made common to three identical switching circuits at A, B and C.

Line Amplifiers

Figure 15A.4B

13 The amplifiers for operator positions LOC, REM1 and REM2 are identical. The LOC line amplifier VT1, VT2, VT3 is described. VT1 is a common emitter amplifier with negative feedback coupled to amplifiers VT2 and VT3.

14 The input is applied to the junction C3, R11 which determines VT1 base bias. The gain is precisely set by the ratio between the load R14 and emitter feedback resistor R15. The output impedance (R out) is determined by R19 and the winding resistance of T1. R out is approximately 220Ω. C7, C8 prevent high-frequency oscillation.

15 The usb input to the amplifier is via attenuator network R1, R2, R3 and diode switch MR1. The attenuator network reduces the audio level from the demodulator to a more convenient level for the line amplifier diode switches. This causes the gain per channel to drop by approximately 6 dB when both usb and lsb channels are switched to the same line amplifier.

Line Monitoring

Figure 15A.4B

16 Any one of the three line amplifier outputs may be switched to the monitor output at PLE21. On the LOC line output the diode switch comprises C10, R20, R21, C11, R22 and MR3 with biasing network R64, R63, which is common to all three switches. The REM1 and REM2 circuits are identical in action to the LOC monitor circuit, MR9 and MR12 being the diode switches.

17 Diode switches MR3, MR9, MR12 are controlled by the right- hand, headset, MONITORING switch 1SJ and by the LOC-REM1- REM2 line selector switch 1SC or 1SE on the RECEIVE USB/DSB or the RECEIVE LSB panel. For instance, with 1SJ on USB/DSB and 1SC to REM1, -30 V is routed to R62 to forward bias MR9 so that the REMOTE 1 line amplifier output is monitored. At the same time the LSB line selector 1SE would normally be set to the other remote position REM2 so that on switching 1SJ to LSB, the REMOTE 2 line amplifier output is monitored.

18 If both line selector switches are set to the same position, say to LOC, then the local line amplifier output can be monitored with the headset MONITORING switch 1SJ at USB/DSB or LSB although the signal may be available on only one channel.

Loudspeaker Amplifier

Figure 15A.4C

19 The usb or lsb channel input is applied to the loudspeaker amplifier by diode switches MR4 and MR5, via VOLUME control 1RV2A.

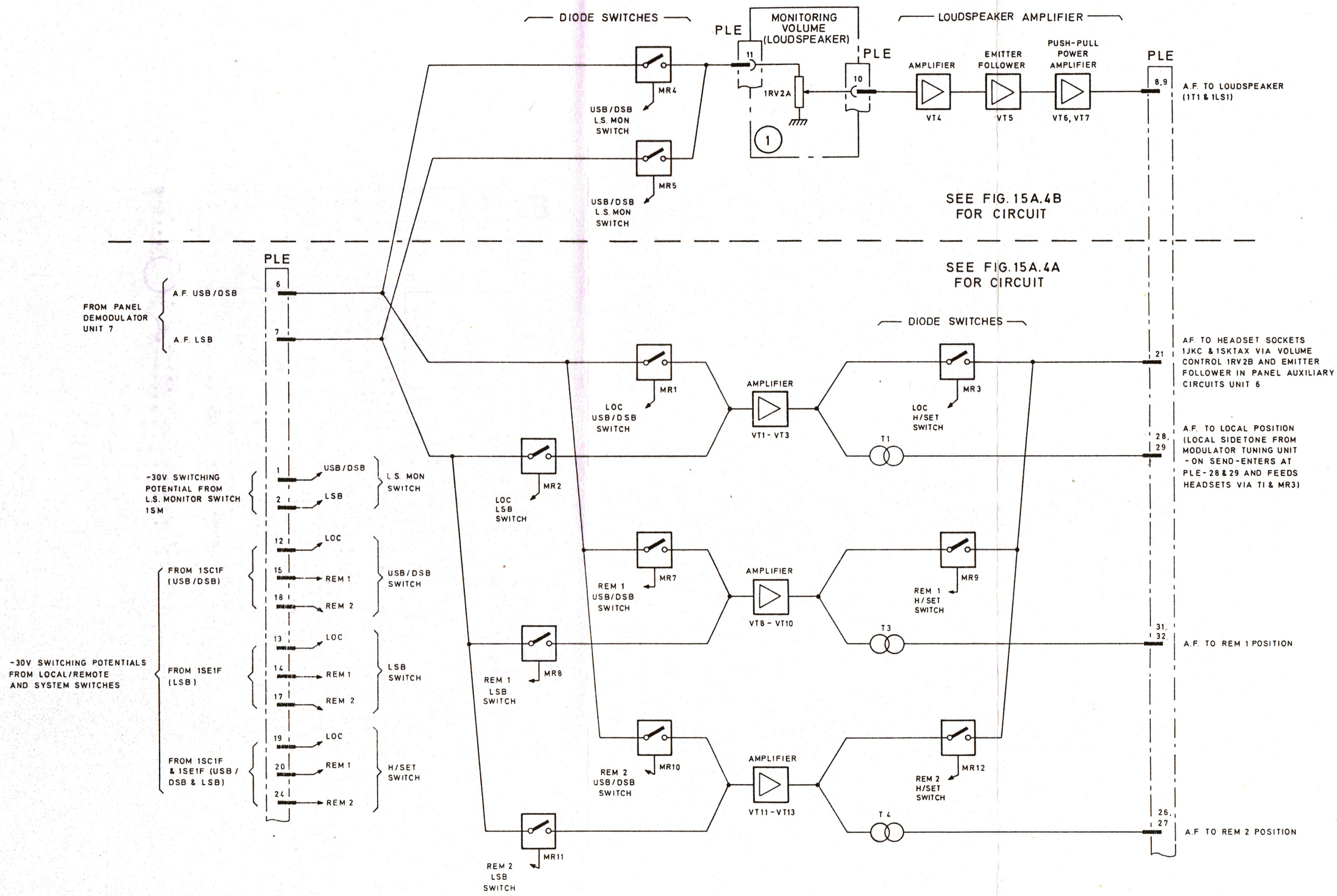
20 The amplifier comprises VT4, VT5, VT6 and VT7. The input is fed to the junction R31, R32, the base bias resistors of VT4. R33 limits the drop in input impedance should the amplifier be overdriven. VT4 is a common emitter stage with feedback, gain being precisely controlled by R35 and R36. VT4 is dc coupled to emitter-follower VT5 which is transformer coupled to the Class B push-pull pair VT6, VT7. C20 inhibits any tendency to high frequency oscillation.

21 VT5 prevents the relatively low input impedance of VT6, VT7 loading VT4 unduly, and provides a low source impedance to the output pair, making it unnecessary to match them.

22 T2 has a 1:1:1 ratio, the centre tapped secondary providing phase opposing drives to VT6 and VT7. The network R30, R40 and MR6 across the +30 V supply applies a small bias, via T2, to VT6 and VT7 which reduces cross-over distortion. MR6 varies the bias voltage with temperature and compensates for the changing requirements of the transistors.

For Link 11 use

23 Board Amplifier Audio Frequency 5820-99-758-9180 must be used together with Panel Demodulator 5820-99-758-9179 and Panel Automatic Gain Control 5820-99-758-9181. Board Amplifier Audio Frequency 5820-99-758-9180 may be used in a normal CJM installation with Panel Automatic Gain Control 5820-99-519-7028 and/or Panel Demodulator 5820-99-519-7029.

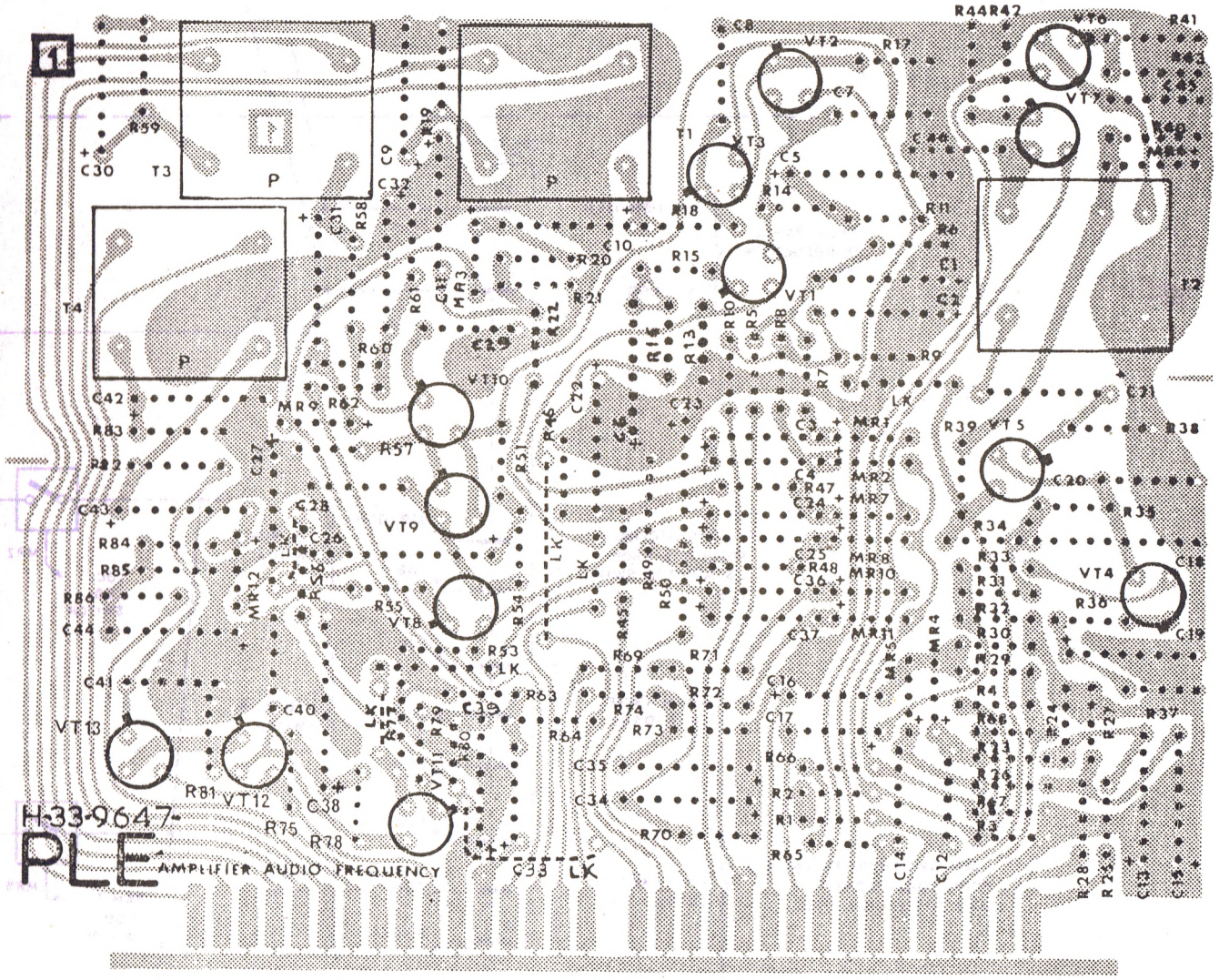


AMPLIFIER AUDIO FREQUENCY 5820-99-758-9180

SUB ASSEMBLY 5A

BLOCK DIAGRAM

FIG 15A. 2



AMPLIFIER AUDIO FREQUENCY
COMPONENT LAYOUT

FIG 15A. 3

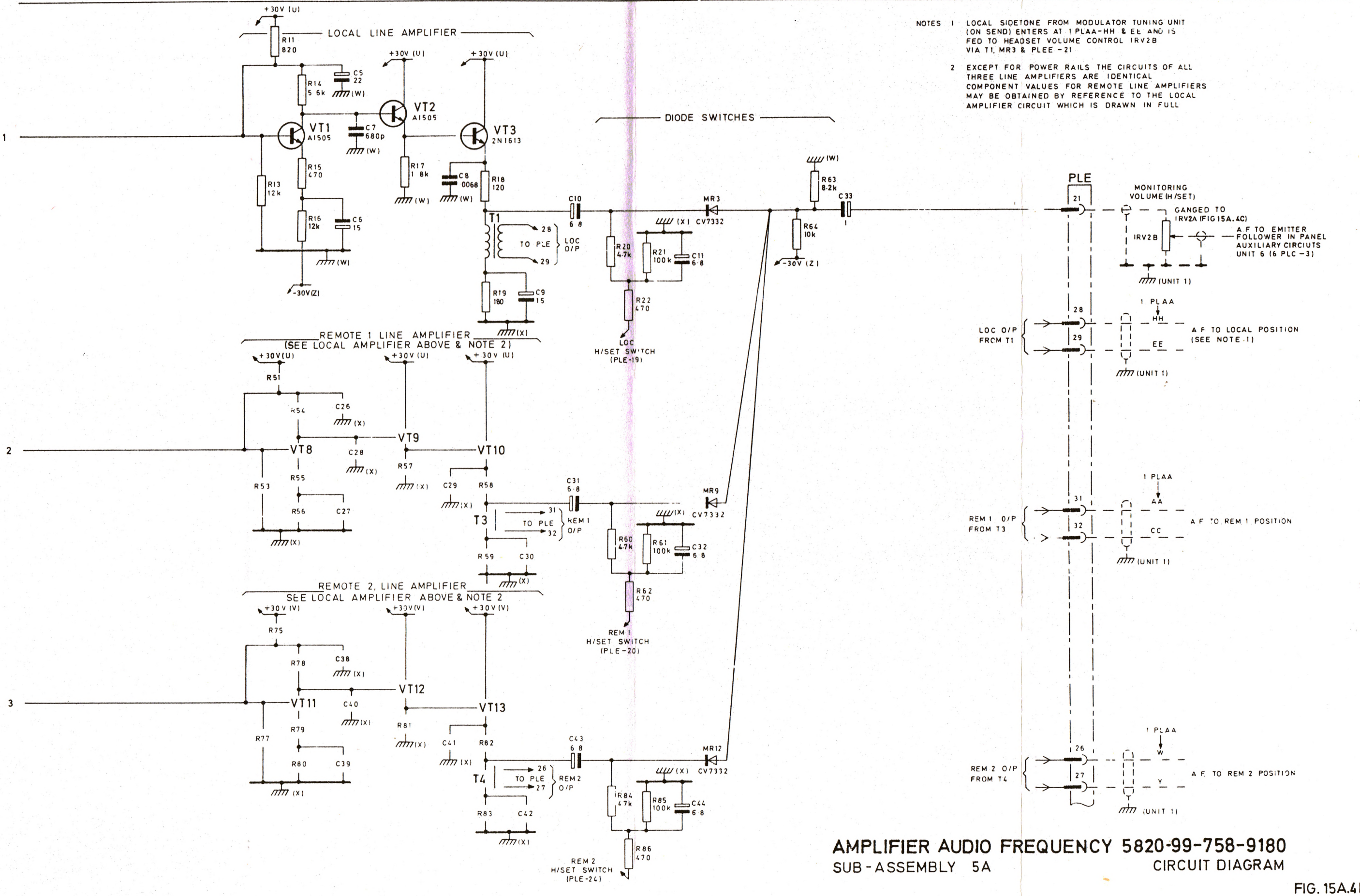
BR4147 (5) A
Amdt. 7.12.84

| | | |

13 53 11 75 14 54 78 79 17 18 58 82 20 22 21 85 63 77 51 15 15 55 56 80 57 81 19 59 83 60 84 62 86 61 64	RES
5 26 38 7 8 9 10 11 6 27 39 28 40 29 41 30 42 31 43 32 44 33	CAP
VT1 VT2 VT3 T1 MR3 VT8 VT11 VT9 VT12 VT10 VT13 T3 T4 MR 9 MR12	MISC

NOTES 1 LOCAL SIDETONE FROM MODULATOR TUNING UNIT (ON SEND) ENTERS AT 1 PLAA-HH & EE AND IS FED TO HEADSET VOLUME CONTROL 1RV2B VIA T1, MR3 & PLEE - 21

2 EXCEPT FOR POWER RAILS THE CIRCUITS OF ALL THREE LINE AMPLIFIERS ARE IDENTICAL COMPONENT VALUES FOR REMOTE LINE AMPLIFIERS MAY BE OBTAINED BY REFERENCE TO THE LOCAL AMPLIFIER CIRCUIT WHICH IS DRAWN IN FULL



AMPLIFIER AUDIO FREQUENCY 5820-99-758-9180

SUB-ASSEMBLY 5A — CIRCUIT DIAGRAM

FIG. 15A.4B

| | | |

CHAPTER 16

PANEL AUTOMATIC GAIN CONTROL

5820-99-519-7028

UNITS 8 AND 9

CONTENTS LIST

	Paragraphs
Introduction	1 - 10
Physical Description	11
Electrical Description	12 - 30
A.G.C. performance	30

TABLES

	Table No
A.G.C. Time Constants	16.1

ILLUSTRATIONS

	Figure No
Panel Automatic Gain Control Block Diagram	16.1
Typical A.G.C. Performance Curves	16.2
Panel Automatic Gain Control Component Layout	16.3
Panel Automatic Gain Control Circuit Diagram	16.4A, B

CHAPTER 16

PANEL AUTOMATIC GAIN CONTROL

5820-99-519-7028

UNITS 8 AND 9

Introduction

Figure 16.1

1. Unit 8 is used for usb, dsb operation. Unit 9 is used for lsb operation. Each panel accepts an input from the appropriate Intermediate Frequency Amplifier (100 kHz) and processes this to produce a d.c. output suitable for use as the A.G.C. control voltage, which is applied to several stages of the I.F. Amplifier (100 kHz) and to the two valve r.f. stages of the Receiver. Each I.F. Amplifier (100 kHz) is controlled only by its appropriate A.G.C. panel, but the A.G.C. to the two r.f. stages is produced by combining the outputs of the two A.G.C. panels so that the control voltage corresponds to the higher level of the two sidebands.

2. The A.G.C. threshold level is such that gain reduction starts to be applied to the I.F. Amplifier with ssb input signals of 1 μV equivalent aerial e.m.f. Overall A.G.C. performance is such that the i.f. output is held constant to within less than 3 dB for input levels between 2 μV and 1 V.

3. Suitable time constants for the different modes of operation are automatically selected by the system switch on the Receiver front panel.

4. On ssb the A.G.C. voltage must be derived from the instantaneous level of the sideband since there is no carrier present. Reception of speech on ssb requires a rapid attack time and fairly long hold time, so that the correct A.G.C. level is reached on the first speech syllable and is maintained during short pauses in the speech.

5. Reception of fst and data on ssb requires a fast attack, short hold and rapid decay time. On dsb the A.G.C. is derived from the carrier and a relatively slow attack and decay time is suitable. Approximate time constants employed are given in Table 16.1.

Table 16.1

A.G.C. Time Constants

Mode	Attack	Recovery
SSB, CW, MCW	5 milliseconds	1 second or 1.7 seconds (selectable)
FST, DATA	5 milliseconds	17 milliseconds
DSB	100 milliseconds	1.5 seconds

6. Separate amplifier, rectifier and time constant filter circuits, selected by the system switch, are used for ssb and dsb reception. The d.c. output from the circuit in use is applied, via emitter followers VT2, VT3, to an A.G.C. reservoir charging circuit VT4, C11 which provides the primary time constant for the long hold and decay times. The surge by-pass circuit R17, C12, MR21 provides for the rapid attack time.

7. Schmitt trigger circuits time the signal and initiate the discharge of A.G.C. reservoir C11. The discharge rate of C11 is controlled via VT15. The hold time is provided by C12, C22 which are selected via the system switch.

8. VT16 is also operated by the trigger circuits to provide a d.c. output to a signal relay used in Outfit CJM. The relay will thus operate when the input signal is above the threshold level and may be used for remote indication purposes or for switching the Receiver output to a relaying transmitter.

9. A control from VT14 to the corresponding Amplifier I.F. (100 kHz) can be applied by the SQUELCH switch on the front panel to mute the receiver if the input signal falls below a certain level. It prevents a.f. noise if pauses in the received signal are long enough for the A.G.C. to decay and restore the receiver to full gain. The squelch threshold level is set about 3 dB below the A.G.C. threshold.

10. The R.F. GAIN control on the front panel or at remote positions applies a d.c. voltage to the A.G.C. lines via VT6. Receiver muting is achieved in the same way.

Physical Description

11. Each unit is a plug-in printed wiring board 7.2 inches by 5.5 inches. A finger pull facilitates removal and slotted guides assist location of the board into its socket. Rubber pads on the printed wiring side prevent it being inserted in the wrong position. Screens on each side are earthed by their mounting pillars.

Electrical Description

Figures 16.2, 16.4A, B

12. VT1 is in use for dsb, VT7 for ssb reception. On USB/DSB with system switch 1SD set to DSB, MR1 is forward biased by -30 V via PLG4 so that VT1 is conducting. With 1SD set to any ssb position, MR12 is forward biased by -30 V via PLG5 so that VT7 is conducting. On LSB, MR12 is forward biased by -30 V via PLH5 so that VT7 is conducting, while PLH4 is not used, putting VT1 out of action.

13. Stages VT1 and VT7 are identical in operation except for the filter circuit time constants. For dsb operation, where the carrier is present, a long time constant is required so C8 is 47 µF. For ssb operation a short time constant is required so C19 is only 0.001 µF.

14. For dsb operation an A.G.C. voltage is required which is dependent on the level of the carrier wave of the received signal. All modulation has to be smoothed out and a d.c. voltage produced which is proportional to the carrier level. This is achieved by VT1, A.G.C. detector MR2 and the associated filter C7, R10, C8. The d.c. voltage is developed across R11. MR3 is a routing diode.

15. For ssb operation an A.G.C. voltage is required which is dependent on the peaks of the received signal because there is no constant carrier wave. This A.G.C. voltage is achieved by VT7, A.G.C. detector MR13 and the associated filter C18, R33, C19. The A.G.C. voltage which is proportional to the peaks of the incoming signal is developed across R11. MR14 is a routing diode.

16. With no signal input there is an A.G.C. delay voltage of +9.5 V on the emitter of VT2, established by R12, R15 across +30 V. As the 100 kHz i.f. input increases towards the reference level of 200 mV (106 dB), the voltage developed across R11 causes VT2 to conduct so that the emitter of VT2 goes to -4.5 V. This is transferred to PLG, H-8 as an A.G.C. voltage of -1.5 V, the difference in voltage being developed across the base-emitter junctions of VT3, VT4, VT5, VT6 and across R23 by the load on the A.G.C. line.

17. With the full input of 400 mV (112 dB) the voltage at the emitter of VT2 is driven to -19.5 V. This appears at PLG, H-8 as an A.G.C. voltage of -12.5 V. A d.c. voltage proportional to the detected signal level is monitored at the collector of VT2 and fed to the front panel meter as the A.G.C. DET. level.

18. VT3 is a low-impedance buffer stage which drives the A.G.C. triggering circuits and the A.G.C. reservoir C11. There are two circuits to be considered, the A.G.C. path to the output of the board and the triggering circuits. The first to be considered is the A.G.C. path to the output.

19. The A.G.C. reservoir C11 has two charging paths. One via VT4 and the other via MR4, MR5 and MR6. R18 in VT4 base circuit limits the current taken through the diodes, so that it is small compared with that through VT4. However, the diodes establish a potential of approximately 1 V across R19, thus controlling the current through VT4 and hence the charge time for C11. This charge time is independent of any charge already existing on C11.

20. R17, MR7, MR9 provide a quick by-pass for VT4 of surges in the input signal, and at the onset of a large signal they reduce the gain of the Receiver until the reservoir capacitor has charged up. C12 provides filtering for the by-pass circuit.

21. C11 is presented with a high-impedance load by emitter-follower VT5 so that when the input signal is cut-off it has a very long discharge time. The A.G.C. voltage is then maintained during pauses in the signal as required for ssb working. In dsb and data operation R20 is switched to shunt C11 so that the A.G.C. voltage falls at a controlled rate when the signal level drops or disappears. PLG16 is switched by the system switch to PLG27 or PLG28 to provide fast or medium discharge path via MR8 when VT15 is switched on by the trigger circuits.

22. R.F. gain control and muting is applied via switching diode MR16 to output stage VT6. VT6 is a power stage which provides a low-impedance drive to the A.G.C. line and the level-setting transistor VT8.

23. The main function of the trigger circuits is to time the signal and, when required, to initiate the discharge of reservoir capacitor C11 and so restore Receiver sensitivity. The trigger circuits also drive squelch circuits on Units 10, 11 and the signal indicating relay RLA, RLB.

24. VT9, VT10 form the first Schmitt trigger which drives timing capacitors C21, C22 via buffer amplifier VT11. With no signal input VT9 is cut-off and VT10 is bottomed so that VT11 base is held at about +2.5 V and VT11 is therefore cut-off. When the signal level reaches threshold level the trigger circuit operates so that VT9 is on, VT10 is cut-off, the base of VT11 goes to approximately -9.5 V and VT11 conducts thus charging C20. The +ve side of C21 is routed to earth via PLG, PLH31 and the system switch on SSB, CW or MCW. C21, C22 control the hold time of the A.G.C. system ie the time between the signal falling below threshold level and C11 starting to discharge. C21 and C22 may be removed from the circuit by breaking link LKA.

25. Without C21 and C22 connected the hold time is approx. 1 second, and with C21 and C22 connected, about 1.7 seconds. On the other system, with only C20 in circuit, the hold time is reduced to a minimum of about 2ms. The threshold, triggering level is set to approximately 3 dB below the onset of A.G.C. This level is +103 dB μV input to the board, or -3 dB μV at the antenna. If the receiver gain is reduced by the R.F. GAIN control, the effective trigger operate level is increased by this amount.

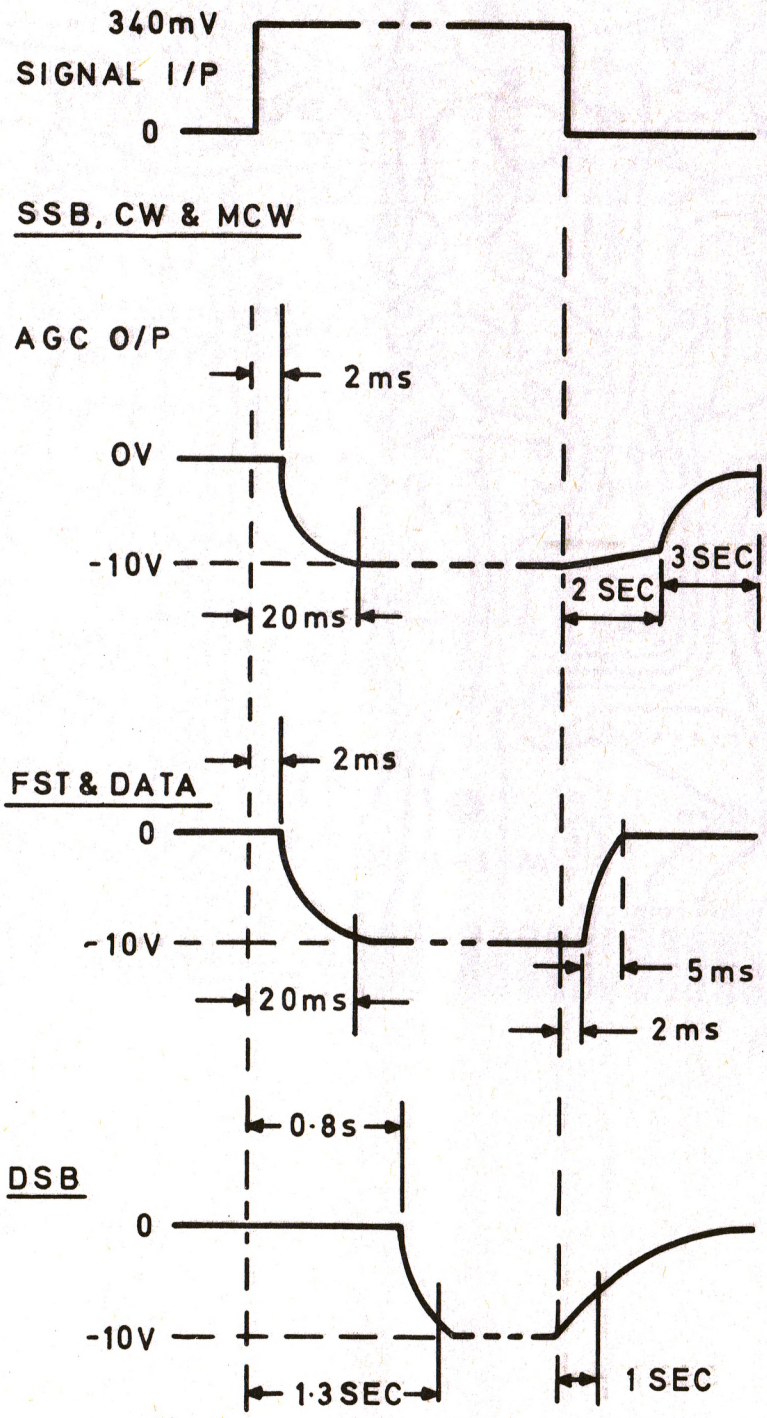
26. The second Schmitt trigger VT12, VT13 has a trigger level set to -2 V. With a d.c. level of -9.0 V at the emitter of VT11, VT13 is held off, keeping VT14 emitter at a level of -19 V. As the voltage on the reservoir capacitor C11 never rises above -14 V, VT15 is cut-off, MR8 is biased off and C11 retains its charge.

27. When the incoming signal disappears or is reduced below the triggering level, circuit VT9, VT10 untriggers so that VT11 returns immediately to about +2.5 V, thus cutting off VT11 so that C21, with C22 if connected, discharges from 9.0 V to earth via R48. When C21 and C22 have discharged to -2 V, VT12 and VT13 untrigger and VT14 emitter drops to +2 V. This allows C11 to discharge through VT15 and whatever resistance is in the discharge path, ie R61, R58 or R61, R59 depending on the position of the system switch. An output is taken from VT15 base for control of squelch circuits.

28. To ensure that VT9, VT10 always reset when the signal level is reduced from its steady level by 3 dB, the trigger operate level has to rise as the signal level rises; otherwise the differential becomes too large. This is achieved by feeding back the A.G.C. voltage from VT6 emitter to VT8 and using the voltage across R37 to vary the trigger operate level.

29. Amplifier VT16 is connected to -30 V when a signal is present. It conducts and operates, in Outfit CJM, a signal relay RLA, RLB to indicate that a signal above the threshold level is present. C23 and MR18 are for spike suppression. The signal relay is not fitted in Type 641 where it is replaced by a resistor.

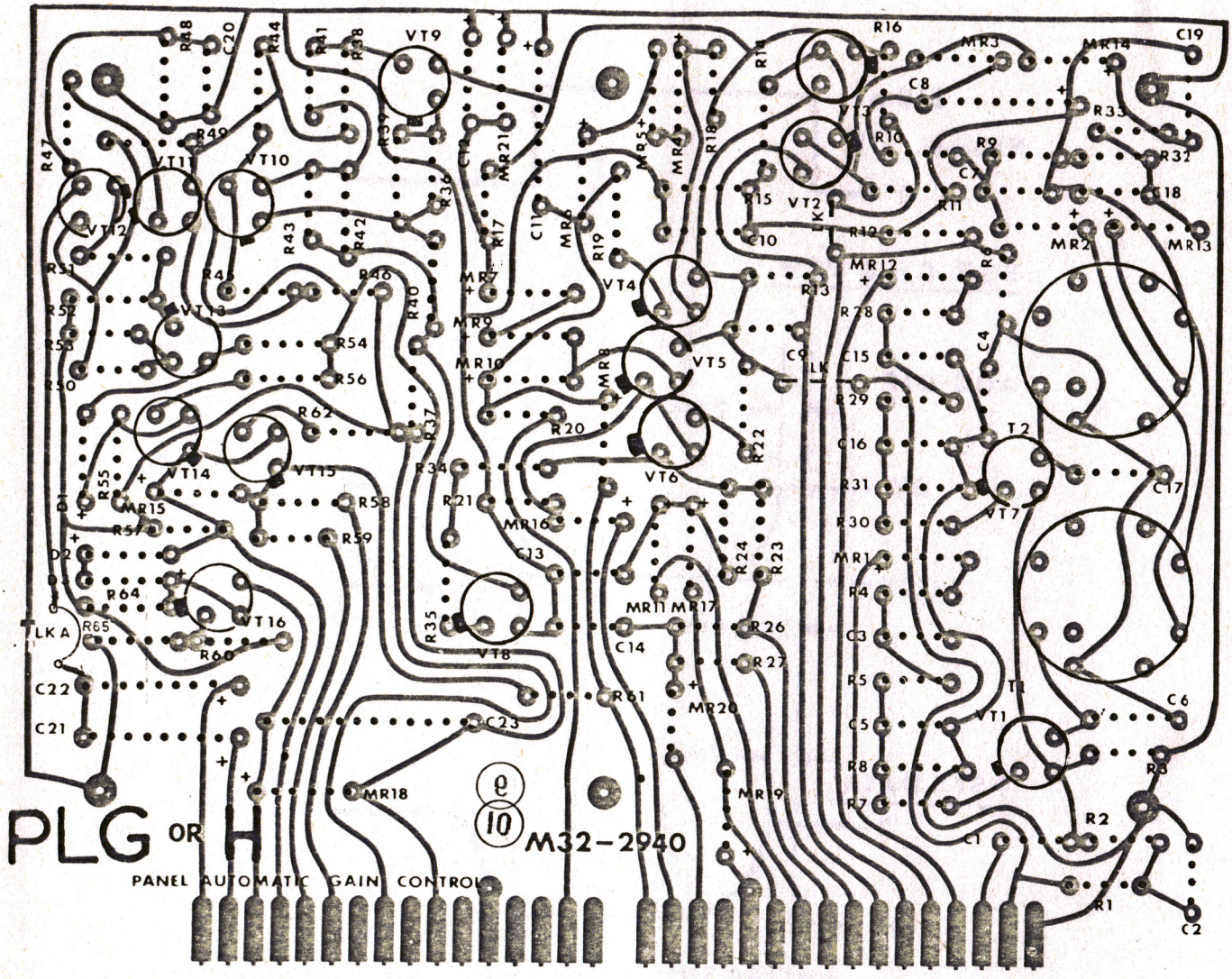
30. A.G.C. performance. The typical curves in Figure 16.2 demonstrate the performance of the Panel Automatic Gain Control when operated, outside the Receiver, with an input from a signal generator suddenly applied and then removed. It should be noted that when the panel is operating in the Receiver it is within the A.G.C. loop so that different conditions will apply. In particular the 'attack' times, when first receiving a signal, are considerably less because the main time constant capacitors will be partially charged by Receiver noise and, apart from the initial signal, the subsequent changes of level will be relatively small so that the full circuit time constants will not be involved. In operation the normal 'attack' times are of the order of 5 ms on all systems except dsb, when it is about 100 ms.



NOTE:- TIMES ARE NOT TO SCALE

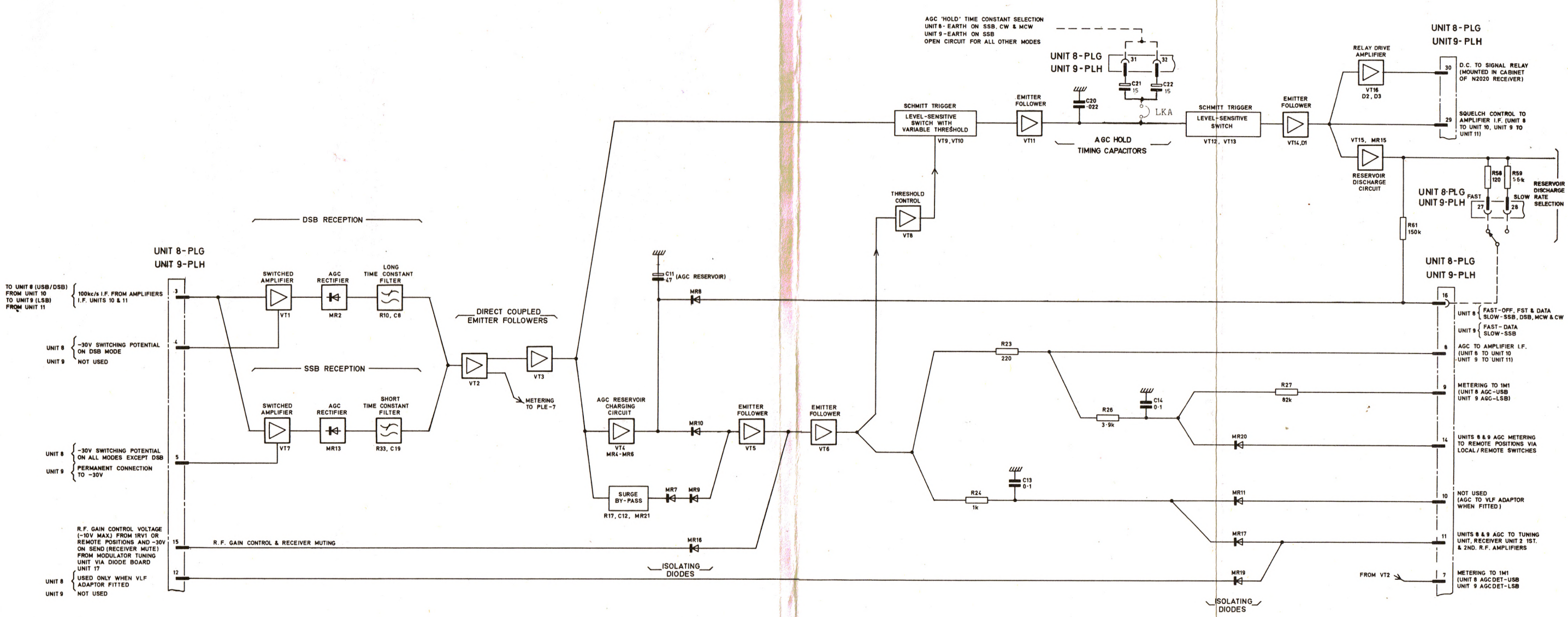
TYPICAL A.G.C. PERFORMANCE CURVES

FIG.16·2



M32-2940 L ISS II

FIG. 16.3 PANEL AUTOMATIC GAIN CONTROL COMPONENT LAYOUT



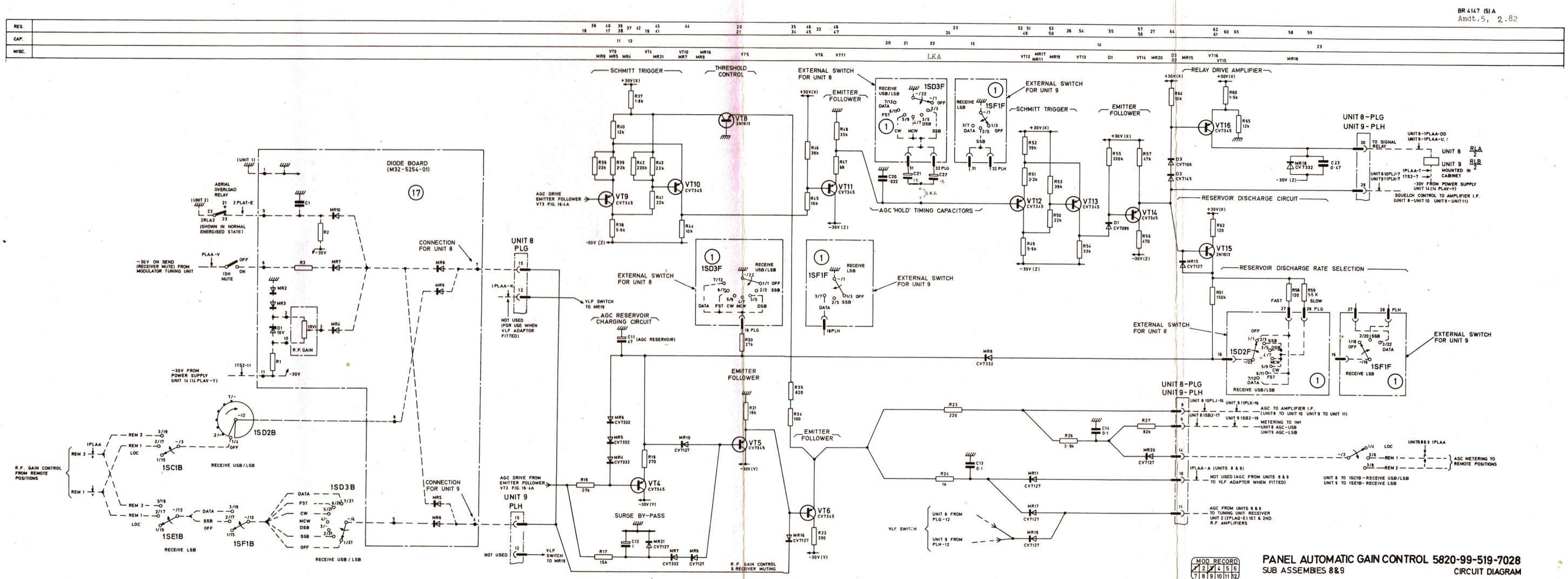
PANEL AUTOMATIC GAIN CONTROL 5820-99-519-7028
SUB ASSEMBLIES 8&9 BLOCK DIAGRAM

FIG16·1

B.R. 4147 (5) A
Amdt.5, 2 .82

| | | |

BR 4147 (5) A
Amdt. 5, 2.82



MOD RECORD
1 2 3 4 5 6
7 8 9 10 11 12

PANEL AUTOMATIC GAIN CONTROL 5820-99-519-7028

SUB ASSEMBIES 8&9

CIRCUIT DIAGRAM

FIG 16-4B

CHAPTER 16A

PANEL AUTOMATIC GAIN CONTROL

5820-99-758-9181

UNITS 8A AND 9A

CONTENTS

Paragraphs

1 Introduction
11 Physical Description
12 Electrical Description
30 AGC Performance
31 For Link 11 use

TABLES

Table

16.1A AGC Time Constants

ILLUSTRATIONS

Figure

16A.1A Panel Automatic Gain Control Block Diagram
16A.1B Panel Automatic Gain Control Block Diagram
16A.2 Typical AGC Performance Curves
16A.3 Panel Automatic Gain Control Component Layout
16A.4A Panel Automatic Gain Control Circuit Diagram
16A.4B Panel Automatic Gain Control Circuit Diagram
16A.4C Panel Automatic Gain Control Circuit Diagram

CHAPTER 16A

PANEL AUTOMATIC GAIN CONTROL

5820-99-758-9181

UNITS 8A AND 9A

Introduction

Figure 16A.1

1 Unit 8A is used for usb, dsb operation. Unit 9A is used for lsb operation. Each panel accepts an input from the appropriate Intermediate Frequency Amplifier (100 kHz) and processes this to produce a d.c. output suitable for use as the AGC control voltage, which is applied to several stages of the IF Amplifier (100 kHz) and to the two valve rf stages of the Receiver. Each IF Amplifier (100 kHz) is controlled only by its appropriate AGC panel, but the AGC to the two valve rf stages is produced by combining the outputs of the two AGC panels so that the control voltage corresponds to the higher level of the two sidebands.

2 The AGC threshold level is such that gain reduction starts to be applied to the IF Amplifier with ssb input signals of 1 µV equivalent aerial emf. Overall AGC performance is such that the if output is held constant to within less than 3 dB for input levels between 2 µV and 1 V.

3 Suitable time constants for the different modes of operation are automatically selected by the system switch on the Receiver front panel.

4 On ssb the AGC voltage must be derived from the instantaneous level of the sideband since there is no carrier present. Reception of speech on ssb requires a rapid attack time and fairly long hold time, so that the correct AGC level is reached on the first speech syllable and is maintained during short pauses in the speech.

5 Reception of fst and data on ssb requires a fast attack, short hold and rapid decay time. On dsb the AGC is derived from the carrier and a relatively slow attack and decay time is suitable. Approximate time constants employed are given in Table 16.1A.

TABLE 16A.1

AGC TIME CONSTANTS

MODE	ATTACK	RECOVERY
SSB: CW, MCW	20 milliseconds	3 second
SSB: FST, DATA	17 milliseconds	17 milliseconds
DSB	0.5 milliseconds	1.5 seconds

6 Separate amplifier, rectifier and time constant filter circuits, selected by the system switch, are used for ssb and dsb reception. The dc output from the circuit in use is applied via emitter followers VT2, VT3, to an AGC reservoir charging circuit VT4, C11 which provides the primary time constant for the long hold and decay times. The surge by-pass circuit R17, C12, MR21 provides for the rapid attack time.

7 Schmitt trigger circuits time the signal and initiate the discharge of AGC reservoir C11. The discharge rate of C11 is controlled via VT15. The hold time is provided by C12, C22 which are selected via the system switch.

8 VT16 is also operated by the trigger circuits to provide a dc output to a signal relay used in Outfit CJM. The relay will thus operate when the input signal is above the threshold level and may be used for remote indication purposes or for switching the Receiver output to a relaying transmitter.

9 A control from VT14 to the corresponding Amplifier IF (100 kHz) can be applied by the SQUELCH switch on the front panel to mute the receiver if the input signal falls below a certain level. It prevents af noise if pauses in the received signal are long enough for the AGC to decay and restore the receiver to full gain. The squelch threshold level is set about 3 dB below the AGC threshold.

10 The RF GAIN CONTROL on the front panel or at remote positions applies a dc voltage to the AGC lines via VT6. Receiver muting is achieved in the same way.

Physical Description

11 Each unit is a plug-in printed wiring board 7.2 inches by 5.5 inches. A finger pull facilitates removal and slotted guides assist location of the board into its socket. Rubber pads on the printed wiring side prevent it being inserted in the wrong position. Screens on each side are earthed by their mounting pillars.

Electrical Description

Figures 16A.2, 16A.4A, 16A.4B

12 VT1 is in use for dsb, VT7 for ssb reception. On USB/DSB with system switch 1SD set to DSB, MR1 is forward biased by -30 V via PLG4 so that VT1 is conducting. With 1SD set to any ssb position, MR12 is forward biased by -30 V via PLG5 so that VT7 is conducting. On LSB, MR12 is forward biased by -30 V via PLH5 so that VT7 is conducting, while PLH4 is not used, putting VT1 out of action.

13 Stages VT1 and VT7 are identical in operation except for the filter circuit time constants. For dsb operation, where the carrier is present, a long time constant is required so C8 is 100 µF. For SSB operation a short time constant is required so C19 is only 0.001 µF.

14 For dsb operation an AGC voltage is required which is dependent on the level of the carrier wave of the received signal. All modulation has to be smoothed out and a dc voltage produced which is proportional to the carrier level. This is achieved by VT1, AGC detector MR2 and the associated filter C7, R10, C8. The dc voltage is developed across R11. MR3 is a routing diode.

15 For ssb operation an AGC voltage is required which is dependent on the peaks of the received signal because there is no constant carrier wave. This AGC voltage is achieved by VT7, AGC detector MR13 and the associated filter C18, R33, C19. The AGC voltage which is proportional to the peaks of the incoming signal is developed across R11. MR14 is a routing diode.

16 With no signal input there is an AGC delay voltage of +9.5 V on the emitter of VT2, established by R12, R15 across +30 V. As the 100 kHz if input increases towards the reference level of 200 mV (106 dB), the voltage developed across R11 causes VT2 to conduct so that the emitter of VT2 goes to -4.5 V. This is developed across the base-emitter junctions of VT3, VT4, VT5, VT6 and across R23 by the load on the AGC line.

17 With the full input of 400 mV (112 dB) the voltage at the emitter of VT2 is driven to -19.5 V. This appears at PLC, H-8 as an AGC voltage of -17V. A dc voltage proportional to the detected signal level is monitored at the collector of VT2 and fed to the front panel meter as the AGC DET. level.

18 VT3 is a low-impedance buffer stage which drives the AGC triggering circuits and the AGC reservoir C11. There are two circuits to be considered, the AGC path to the output of the board and the triggering circuits. The first to be considered is the AGC path to the output.

19 The AGC reservoir C11 has two charging paths. One via VT4 and the other via MR4, MR5 and MR6. R18 in VT4 base circuit limits the current taken through the diodes, so that it is small compared with that through VT4. However, the diodes establish a potential of approximately 1V across R19, thus controlling the current through VT4 and hence the charge time for C11. This charge time is independent of any charge already existing on C11. R66 is added to complete the emitter path to earth.

20 R17, MR7, MR9 provide a quick by-pass for VT4 of surges in the input signal, and at the onset of a large signal they reduce the gain of the Receiver until the reservoir capacitor has charged up. C12 provides filtering for the by-pass circuit.

21 C11 is presented with a high impedance load by emitter-follower VT5 so that when the input signal is cut-off it has a very long discharge time. The AGC voltage is then maintained during pauses in the signal as required for ssb working. In dsb and data operation R20 is switched to shunt C11 so that the AGC voltage falls at a controlled rate when the signal level drops or disappears. PLG16 is switched by the system switch to PLG27 or PLG28 to provide fast or medium discharge path via MR8 when VT15 is switched on by the trigger circuits.

22 RF gain control and muting is applied via switching diode MR16 to output stage VT6. VT6 is a power stage which provides a low-impedance drive to the AGC line and the level-setting transistor VT8.

23 The main function of the trigger circuits is to time the signal and, when required, to initiate the discharge of reservoir capacitor C11 and so restore Receiver sensitivity. The trigger circuits also drive squelch circuits on units 10 11 and the signal indicating relay RLA, RLB.

24 VT9, VT10 form the first Schmitt trigger which drives timing capacitors C21, C22 via buffer amplifier VT11. With no signal input VT9 is cut-off and VT10 is bottomed so that VT11 base is held at about +2.5 V and VT11 is therefore cut-off. When the signal level reaches threshold level the trigger circuit operates so that VT9 is on, VT10 is cut-off, the base of VT11 goes to approximately -9.5 V and V11 conducts thus charging C20. The +ve side of C21 is routed to earth via PLG, PLH31 and the system switch on SSB, CW or MCW. C21, C22 control the hold time of the AGC system ie the time between the signal falling below threshold level and C11 starting to discharge. C21 and C22 may be removed from the circuit by breaking link LKA.

25 Without C21 and C22 connected the hold time is approximately 1 second, and with C21 and C22 connected, about 1.7 seconds. On the other system, with only C20 in circuit, the hold time is reduced to a minimum of about 2 ms. The threshold, triggering level is set to approximately 7 dB below the onset of AGC. This level is +90 dB µV input to the board, or -3 dB µV at the antenna. If the receiver gain is reduced by the RF GAIN control, the effective trigger operate level is increased by this amount.

26 The second Schmitt trigger VT12, VT13 has a trigger level set to -2 V. With a dc level of -9.0 V at the emitter of VT11, VT13 is held off, keeping VT14 emitter at a level of -19 V. As the voltage on the reservoir capacitor C11 never rises above -14 V, VT15 is cut-off, MR8 is biased off and C11 retains its charge.

27 When the incoming signal disappears or is reduced below the triggering level, circuit VT9, VT10 untriggers so that VT11 returns immediately to about +2.5 V, thus cutting off VT11 so that C21, with C22 if connected, discharges from 9.0 V to earth via R48. When C21 and C22 have discharged to -2 V, VT12 and VT13 untrigger and VT14 emitter drops to +2 V. This allows C11 to discharge through VT15 and whatever resistance is in the discharge path, ie R61, R58 or R61, R59 depending on the position of the system switch. An output is taken from VT15 base for control of squelch circuits.

28 To ensure that VT9, VT10 always reset when the signal level is reduced from its steady level by 7 dB, the trigger operate level has to rise as the signal level rises; otherwise the differential becomes too large. This is achieved by feeding back the AGC voltage from VT6 emitter to VT8 and using the voltage across R37 to vary the trigger operate level.

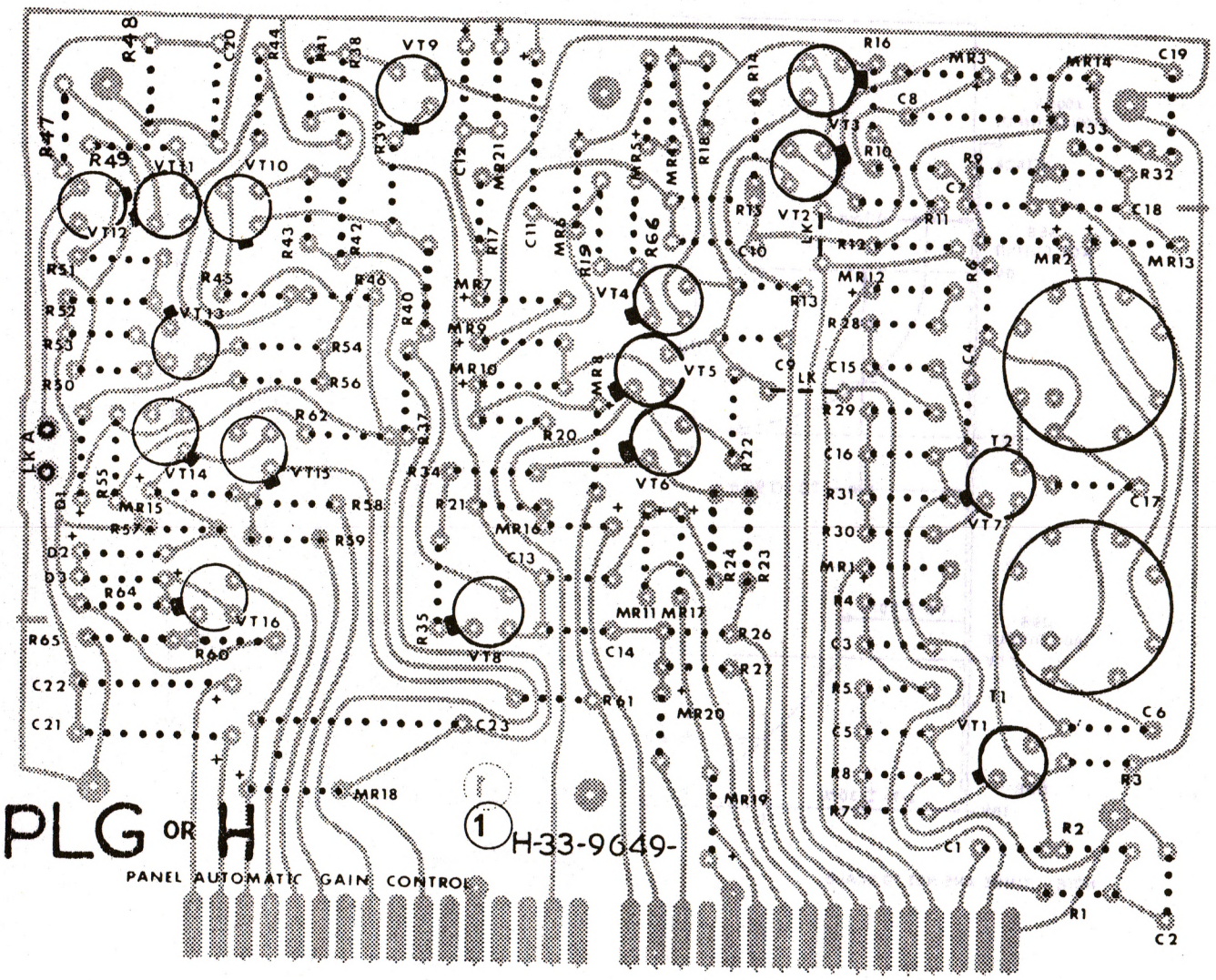
29 Amplifier VT16 is connected to -30 V when a signal is present. It conducts and operates, in Outfit CJM, a signal relay RLA, RLB to indicate that a signal above the threshold level is present. C23 and MR18 are for spike suppression. The signal relay is not fitted in Type 641 where it is replaced by a resistor.

AGC Performance

30 The typical curves in Figure 16A.2 demonstrate the performance of the Panel Automatic Gain Control when operated, outside the receiver, with an input from a signal generator suddenly applied and then removed. It should be noted that when the panel is operating in the Receiver it is within the AGC loop so that different conditions will apply. In particular the 'attack' times, when first receiving a signal, are considerably less because the main time constant capacitors will be partially charged by Receiver noise and, apart from the initial signal, the subsequent changes of level will be relatively small so that the full circuit time constants will not be involved. In operation the normal 'attack' times are of the order of 20 ms on all systems except dsb, when it is about 0.5 seconds.

For Link 11 use

31 Panel Automatic Gain Control 5820-99-758-9181 must be used together with Panel Demodulator 5820-99-758-9179 and Board Amplifier Audio Frequency 5820-99-758-9180. Panel Automatic Gain Control 5820-99-758-9181 may be used in a normal CJM installation with Amplifier Audio Frequency 5820-99-519-7030 and/or Panel Demodulator 5820-99-519-7029.



PANEL AUTOMATIC GAIN CONTROL
COMPONENT LAYOUT

FIG 16A.3

UNIT 8 - PLG
UNIT 9 - PLH

1TS1-4
1TS-6
(UNIT 1)
PLH - 4 IS NOT USED ON UNIT 9
OARD
CTIONS FOR ONLY
ECTION FOR ONLY
18

+30V(W)
+30V(X)
-30V(Y)
-30V(Z)

R6 1k
C4 0·1
R3 8·2k
C1 0·1
R2 82k
C2 0·1
R1 15k
-30V(Y)
C3 0·1
C5 0·1
R8 100k
MR1 CV7332
R4 2·2k
R5 2·2k
R7 150
R30 150
C15 0·1
C16 0·1
R31 100k
MR12 CV7332
R28 2·2k
R29 2·2k

DSB RECEPTION
SWITCHED AMPLIFIER
AGC RECTIFIER
LONG TIME CONSTANT FILTER
T1
C6 ·0015
MR2 CV7127
R9 6·8k
C7 ·01
R10 22k
C8 47
MR3 CV7127
VT1 A1826

SSB RECEPTION
SWITCHED AMPLIFIER
AGC RECTIFIER
SHORT TIME CONSTANT FILTER
T2
C17 ·0015
MR13 CV7127
R32 6·8k
C18 ·01
R33 22k
C19 ·001
MR14 CV7127
VT7 A1826

DIRECT COUPLED EMITTER FOLLOWERS
+30V(W)
R12 56k
R14 8·2k
R15 27k
C10 ·0015
R16 12k
R11 220k
VT3 CV7345
VT2 CV7345
-30V(Y)
R13 120
C9 0·1

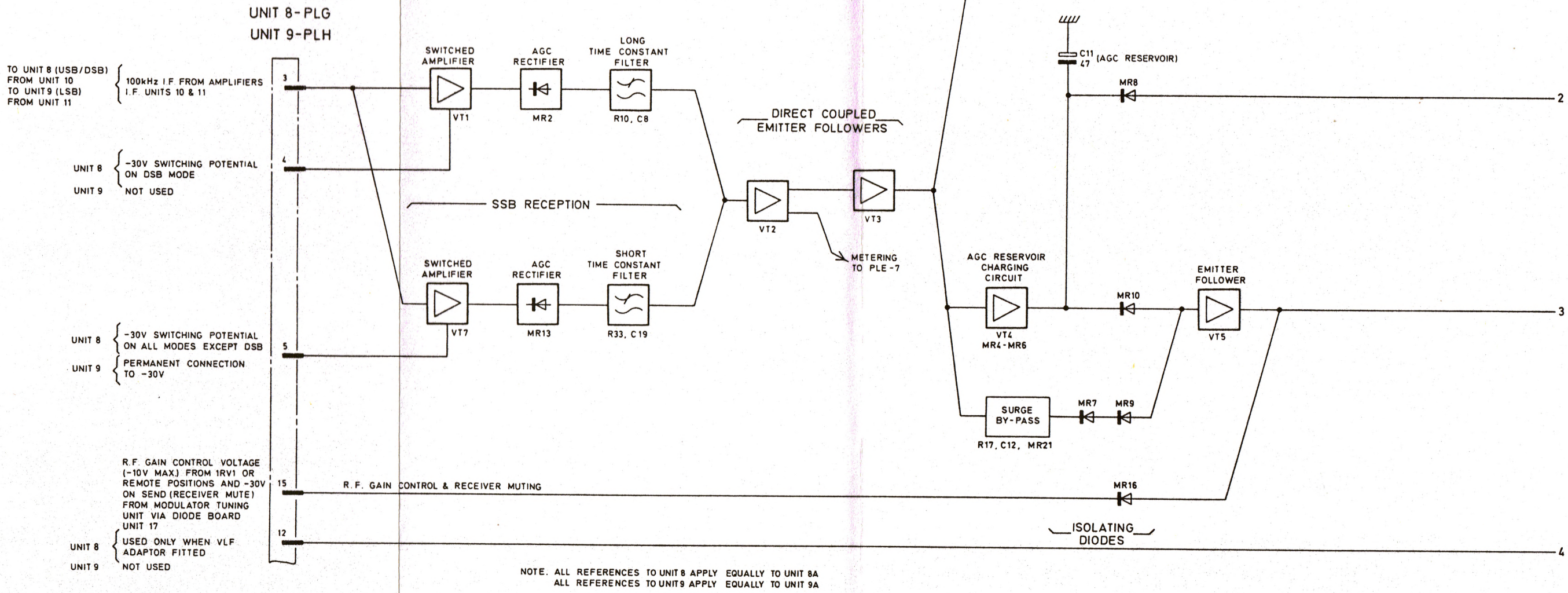
AGC DRIVE TO SCHMITT TRIGGER VT3 (FIG. 16A.4B)
AGC DRIVE TO RESERVOIR CHARGING CIRCUIT R13/VT4 (FIG. 16A.4B)
UNIT 8 - PLG
UNIT 9 - PLH
UNIT 8 1SB1F-13
UNIT 9 1SB1F-15
METERING TO 1M1
UNIT 8 AGC DET - USB
UNIT 9 AGC DET - LSB

REFERENCES TO UNIT 8 APPLY EQUALLY TO UNIT 8A
REFERENCES TO UNIT 9 APPLY EQUALLY TO UNIT 9A

PANEL AUTOMATIC GAIN CONTROL 5820-99-758-9181
SUB-ASSEMBLIES 8A & 9A
CIRCUIT DIAGRAM

FIG. 16A.4A

| | | |

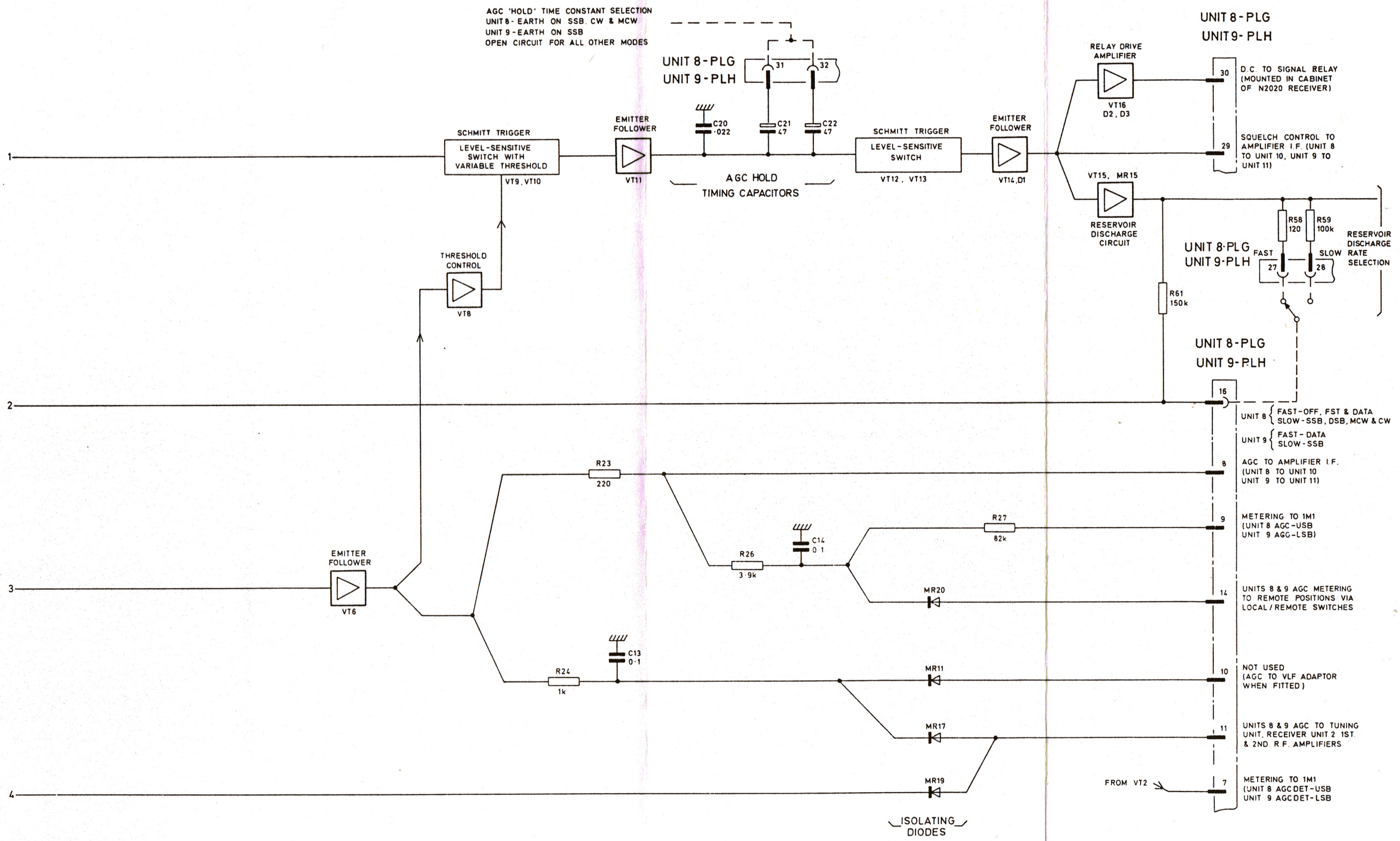


NOTE. ALL REFERENCES TO UNIT 8 APPLY EQUALLY TO UNIT 8A
ALL REFERENCES TO UNIT 9 APPLY EQUALLY TO UNIT 9A

PANEL AUTOMATIC GAIN CONTROL 5820-99-758-9181

SUB ASSEMBLIES 8A & 9A BLOCK DIAGRAM

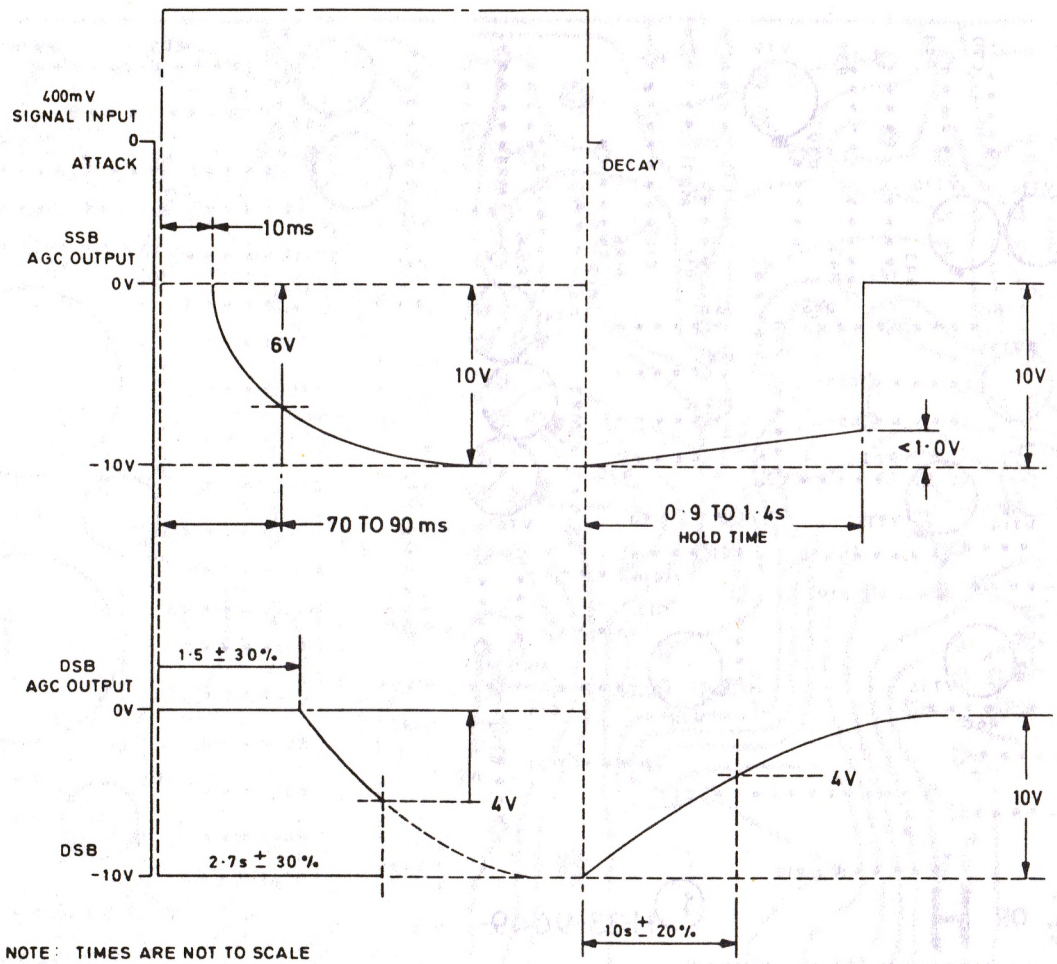
FIG 16A.1A



PANEL AUTOMATIC GAIN CONTROL 5820-99-758-9181

SUB ASSEMBLIES 8A & 9A — BLOCK DIAGRAM

FIG 16A.1B



NOTE: TIMES ARE NOT TO SCALE

TYPICAL A G C PERFORMANCE CURVES FIG. 16 A.2

BR4147(5)A
Amdt 7,12,84

| | | |

35 34 46 45 22 48 47 23 24 52 51 49 53 50 26 54 55 57 56 27 64 62 61 60 65 58 59	RES
20 21 22 13 14 23	CAPS
VT6 VT11 VT12 MR17 MR11 MR19 VT13 D1 VT14 MR20 D3 D2 MR15 VT16 VT15 MR18	MISC

EXTERNAL SWITCH FOR UNIT 8

EMITTER FOLLOWER

+30V(X)

R48 33k

R47 68

R46 39k

R45 10k

VT11 CV7345

-30V(Z)

RECEIVE USB/LSB

1SD3F

7/12 DATA

6/11 FST

5/9

3/5 4/7 DSB

2/3

-/22

-/1

OFF

CW MCW SSB

31 32 PLG

C20 ·022

C21 47

C22 47

EXTERNAL SWITCH FOR UNIT 9

RECEIVE LSB

1SF1F

-/1

3/7 DATA

1/3 2/5 SSB OFF

31 32 PLH

SCHMITT TRIGGER

+30V(X)

R52 39k

R51 2·2k

R53 39k

R50 22k

R49 5·6k

R54 33k

VT12 CV7345

VT13 CV7345

-30V(Z)

AGC 'HOLD' TIMING CAPACITORS

EMITTER FOLLOWER

+30V(X)

R55 330k

R57 47k

D1 CV7099

VT14 CV7345

R56 470

-30V(Z)

RELAY DRIVE AMPLIFIER

+30V(X)

R64 10k

R60 1·5k

VT16 CV7345

R65 12k

D3 CV7106

D2 CV7145

MR18 CV7332

C23 0·47

-30V(Z)

RESERVOIR DISCHARGE CIRCUIT

+30V(X)

R62 120

VT15 2N1613

MR15 CV7127

RESERVOIR DISCHARGE RATE SELECTION

R61 150k

R58 120 FAST

R59 100k SLOW

EXTERNAL SWITCH FOR UNIT 8

1SD2F

OFF

1/1

2/3 SSB

3/5 DSB

4/7

MCW

5/9 CW

6/11 FST

7/12 DATA

-/22

RECEIVE USB/LSB

27 28 PLG

16

EXTERNAL SWITCH FOR UNIT 9

1SF1F

1/18 OFF

2/20 SSB

3/22 DATA

-/16

RECEIVE LSB

27 28 PLH

16

UNIT 8 - PLG
UNIT 9 - PLH

30 TO SIGNAL RELAY

UNIT 8 - 1PLAA-DD
UNIT 9 - 1PLAA-U

UNIT 8 RLA/2
UNIT 9 RLB/2
MOUNTED IN CABINET

1PLAA-T
1TS2-7

-30V FROM POWER SUPPLY UNIT 14 (14 PLAV-Y)

UNIT 8 10PLJ-7
UNIT 9 11PLK-7

29

SQUELCH CONTROL TO AMPLIFIER I F (UNIT 8 - UNIT 10 UNIT 9 - UNIT 11)

1 2 3 4 5

EMITTER FOLLOWER

R21 18k

VT5 CV7345

-30V(Y)

R35 1k

R34 180

EMITTER FOLLOWER

R23 220

R26 3·9k

C14 0·1

R27 82k

MR20 CV7127

R24 1k

C13 0·1

MR11 CV7127

MR17 CV7127

MR19 CV7127

VT6 CV7345

MR16 CV7127

R22 330

-30V(Y)

VLF SWITCH

UNIT 8 FROM PLG-12

UNIT 9 FROM PLH-12

R.F. GAIN CONTROL & RECEIVER MUTING

MR8 CV7332

UNIT 8 - PLG
UNIT 9 - PLH

8 UNIT 8 10PLJ-16 UNIT 9 11PLK-16 AGC TO AMPLIFIER I.F. (UNIT 8 TO UNIT 10 UNIT 9 TO UNIT 11)

9 UNIT 8 1SB2-17 UNIT 9 1SB2-19 METERING TO 1M1 UNIT 8 AGC - USB UNIT 9 AGC - LSB

14 1PLAA-A (UNITS 8 & 9) NOT USED (AGC FROM UNITS 8 & 9 TO VLF ADAPTOR WHEN FITTED)

10

11 AGC FROM UNITS 8 & 9 TO TUNING UNIT RECEIVER UNIT 2 (2PLAQ-E) 1ST & 2ND R.F. AMPLIFIERS

UNITS 8 & 9 1PLAA

1/4 LOC

2/6 REM 1

3/8 REM 2

-/2

AGC METERING TO REMOTE POSITIONS

UNIT 8 TO 1SC1B - RECEIVE USB/LSB
UNIT 9 TO 1SE1B - RECEIVE LSB

PANEL AUTOMATIC GAIN CONTROL 5820-99-758-9181

SUB ASSEMBLIES 8A & 9A — CIRCUIT DIAGRAM

FIG 16A.4C

CHAPTER 17

PANEL SERVO SUPPLY 5820-99-519-6986

UNIT 4

CONTENTS LIST

	Paragraphs
Introduction	1 - 6
Physical Description	7, 8
Electrical Description	9 - 15

ILLUSTRATIONS

	Figure No
Panel Servo Supply Block Diagram	17.1
Panel Servo Supply Component Layout	17.2
Panel Servo Supply Circuit Diagram	17.3A, B

CHAPTER 17

PANEL SERVO SUPPLY 5820-99-519-6986

UNIT 4

Introduction

Figure 17.1

1. The Panel Servo Supply produces the 400 Hz reference supply and the control voltage for a servo motor in the Tuning Unit.

2. Unit 5 in Modulator Tuning Unit 5820-99-519-6983 is identical.

3. The servo motor control voltage is determined by the difference between a voltage picked off from a potentiometer in the Frequency Synthesiser and a voltage picked off from a feedback potentiometer associated with the servo motor in the Tuning Unit Receiver.

4. The output of a Wien Bridge 400 Hz oscillator VT1, VT2 is amplified and provides the reference phase to the two-phase a.c. motor in the Tuning Unit, Receiver.

5. The output of the reference phase amplifier is also applied to a 90 degrees phase-shift network and then to a chopper modulator VT8. The amplitude of VT8 output will depend on the magnitude of the difference between the two d.c. voltages picked off by the Frequency Synthesiser potentiometer and the motor feedback potentiometer. The phase of VT8 output is determined by the resultant polarity of the d.c. error signal.

6. The resultant a.c. will therefore lead or lag the reference supply by 90 degrees. This signal is amplified by the control phase amplifier and fed out on PLD28, PLD30. The phase of the output will determine the direction of rotation and the amplitude of the output will determine the speed of the motor.

Physical Description

7. Unit 4 is a plug-in printed wiring board 7.2 inches by 5.5 inches. A finger-pull facilitates removal and slotted guides assist location of the panel into its socket. Rubber pads on the printed wiring side prevent it being inserted in the wrong position.

8. One preset potentiometer, adjusted during initial setting-up, is mounted on the panel. Eleven test points are provided on the component side.

Electrical Description

Figure 17.3A, B

9. The output from the 400 Hz Wien Bridge oscillator VT1, VT2 is fed to phase splitter VT3 which drives reference phase amplifiers VT4, VT6 and VT5, VT7 which have input impedances high enough not to load VT3.

10. To satisfy the servo-motor limit parameters, the output stage is designed to operate from $\pm$ 22 V supplies, the source of which depends on whether the Panel Servo Supply is used in a Modulator-Tuning Unit or a Receiver. In the Receiver the -22 V (low) supply at PLD11 is derived from the -41 V unstabilised supply via Panel Receiver Auxiliary Circuits, Unit 6, and the +22 V (high) supply at PLD9 is from Earth. The output load is the centre-tapped reference winding which is tuned to 400 Hz by C11, C12 which ensures maximum power transfer with no need to change the phase.

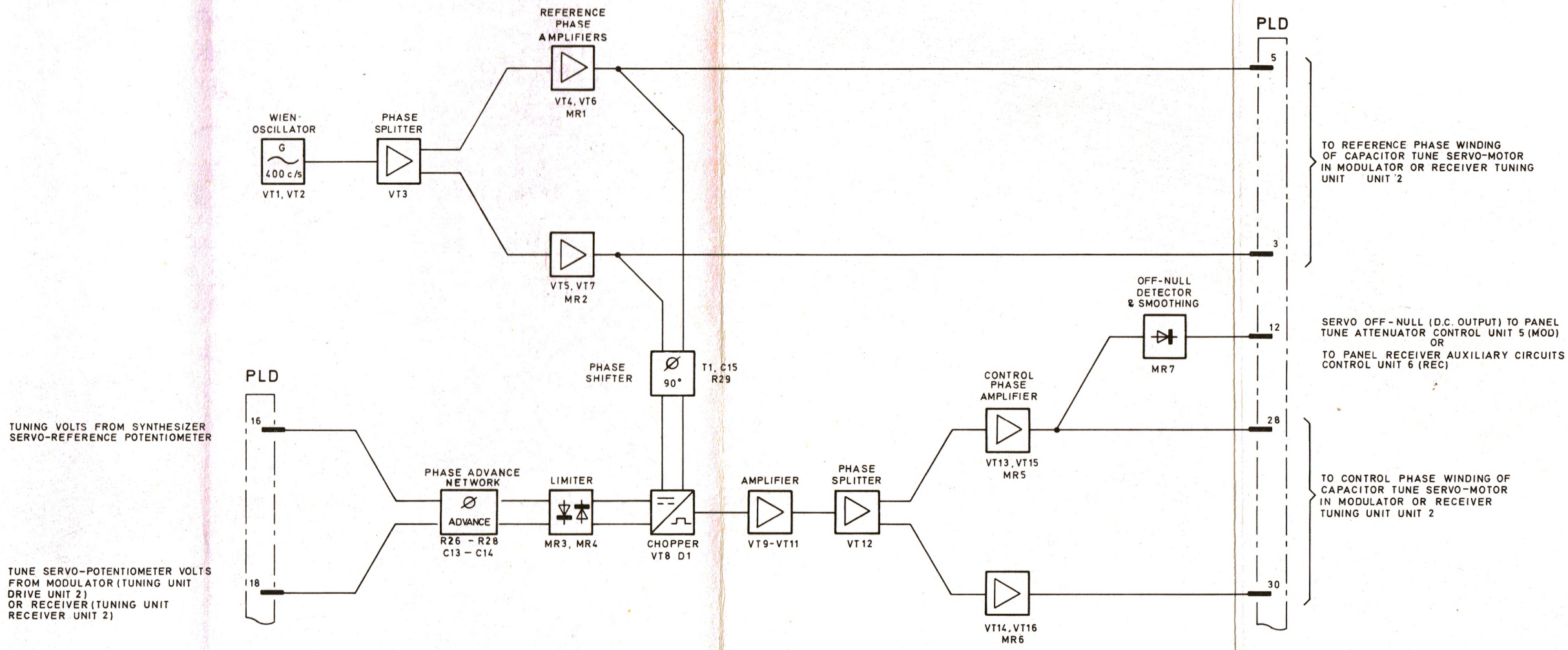
11. The output from VT6, VT7 is also applied to T1 the centre-tapped secondary of which, with R29 and C15, forms a 90 degree phase-shift network. The signal is then limited by D1 and fed as the switching voltage to chopper modulator VT8.

12. The output from VT8 is determined by the voltage between PLD18 and PLD16 ie the difference between the voltage from the servo-motor feedback potentiometer and the voltage from the Synthesiser potentiometer.

13. VT8 output is fed via RV1 to the direct-coupled amplifier VT9, VT10, VT11 followed by phase splitter VT12 which drives the control phase amplifier VT13, VT14. This is identical to the reference phase amplifier and it is supplied with 22 V from the same source via PLD24, 22.

14. The gain of the control-phase amplifier VT13 to VT16 is such that the servo motor develops half torque when the two inputs to the chopper differ by more than 30 mV.

15. The output of the control-phase amplifier is also fed to a servo null detector circuit comprising MR7 and associated components. The positive (with respect to -30 V) voltage output from this detector varies between the approximate limits of 7 V when the motor is driving and 3 V when the servo is at null. This voltage is used in the tune interlock system.

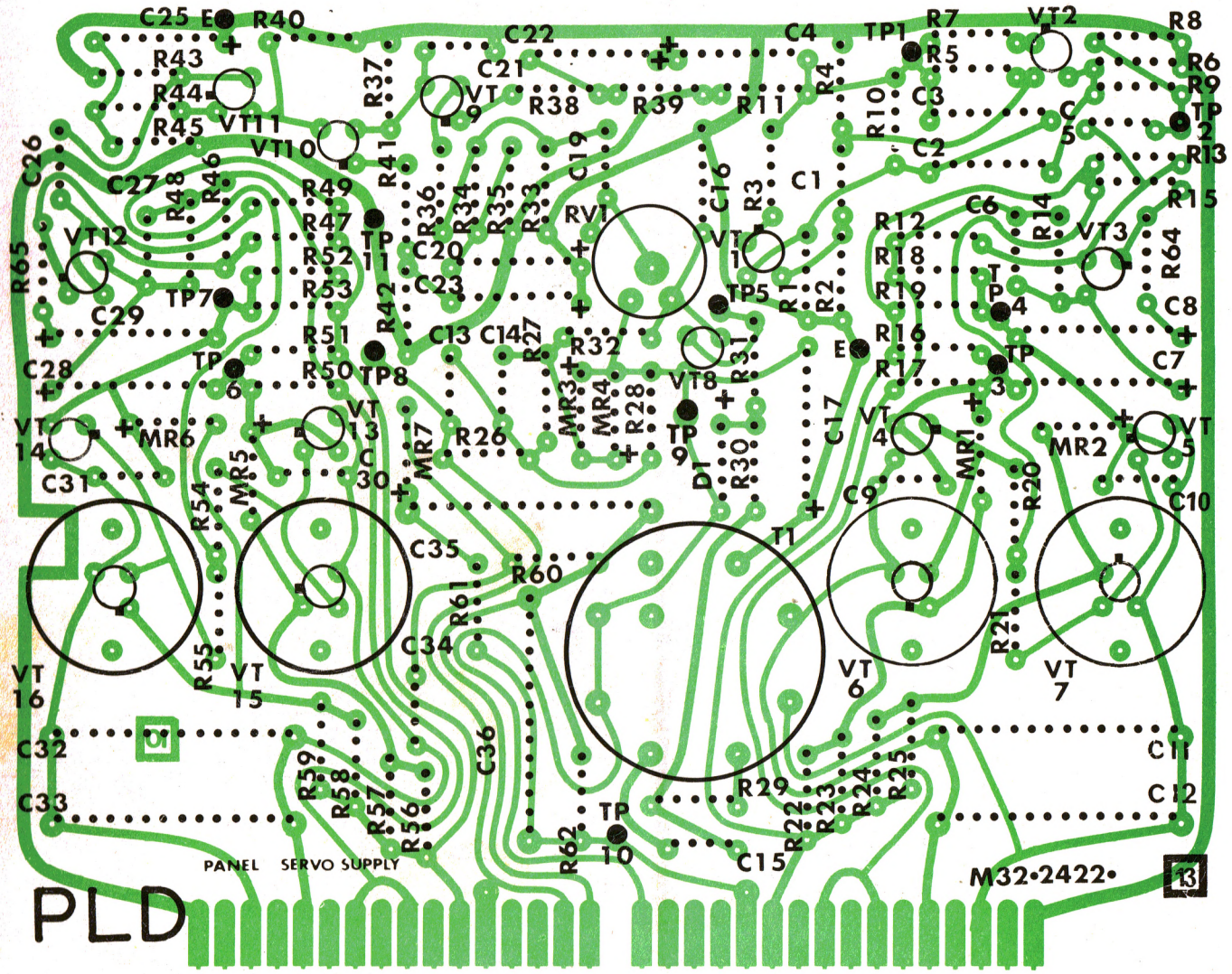


PANEL SERVO SUPPLY 5820-99-519-6986

SUB-ASSEMBLY 4

BLOCK DIAGRAM

FIG. 17·1



M32•2422 [L] ISS 13

FIG. 17.2 PANEL SERVO SUPPLY COMPONENT LAYOUT

14 15 | 64 | 26 | 28 | 17 18 | 27 | 16 19 | 20 21 | 23 24 | 22 25 | 29 | 30 | 32 | 31 | RV1

6 | 13 | 7 8 | 14 | 9 10 | 11 | 15 | 12 | 16 | 17 | 19

VT3 | MR1 MR2 | MR3 MR4 | VT4 VT5 | VT6 VT7 | T1 | D1 | VT8

REFERENCE PHASE AMPLIFIER

22V MOTOR SUPPLY (HIGH)
R17 33K
C9 ·01
TP3
VT4 A1505
MR1 CV7322
VT6 BFY50
R16 1·5K
R20 4·7K
R23 10
R22 10
22V MOTOR SUPPLY (LOW)

ASE SPLITTER
UPPLY (HIGH)
R14 560
C6 0·1
C7 22
VT3 A1505
R64 560
C8 22
R13 22K
R15 1K
SUPPLY (LOW)

22V MOTOR SUPPLY (HIGH)
R18 33K
C10 ·01
TP4
VT5 A1505
MR2 CV7322
VT7 BFY50
R19 1·5K
R21 4·7K
R24 10
R25 10
22V MOTOR SUPPLY (LOW)

PLD
SEE TABLE 1 FOR CONNECTIONS
5
YELLOW
7
GREEN
3
WHITE
CAPACITOR TUNE SERVO-MOTOR REFERENCE WINDING
C11 1·5
C12 1·5
22V MOTOR SUPPLY (HIGH)

BASE VIEWS

B C E — A1505 E1096 BC109 — VT1–VT5 VT8–VT14

E B C — BFY50 — VT6 & VT7 VT15 & VT16

3 4 2 5 1 6 8 7 — T1

PHASE ADVANCE NETWORK
LIMITER
ING VOLTS
TP9
R28 2·2M
MR3 CV7332
MR4 CV7332
R26 47K
C13 0·22
R27 47K
C14 0·22
TP8

90° PHASE SHIFTER
CHOPPER
T1
6 3 1,2 4 5 7
C15 ·047
D1 CV7141 4·3V
R30 47K
R31 22K
TP5
VT8 E1096
R29 4·7K
C16 ·001
R32 120K
RV1 100K
C19 0·22
CHOPPED ERROR SIGNAL TO R36/ VT9 (FIG. 17·3B)
C17 6·8

TABLE 1 – LEAD DESTINATIONS

MODULATOR TUNING UNIT 5820-99-519-6983		RECEIVER 5820-99-519-7019
PLD	MOD. (UNIT 6)	REC. (UNIT 4)
1	EARTH	EARTH
3	2 PLDN-H	2 PLAR-A
5	2 PLDN-J	2 PLAR-B
7	2 PLDN-K	2 PLAR-C
9	1SKTR-Y	EARTH
11 & 22	1SKTR-W	16 PLC-21
12	5PLC-5	6PLC-8
16	1 PLDE-A (VIA 1RLA4)	1PLAA-L
17	1C4 & 4PLR-E & F	1TS2-4
18	2PLDN-P	2PLAR-P
24	1SKTR-W	EARTH
26	2PLDN-L	2PLAR-D
28	2PLDN-M	2PLAR-E
30	2PLDN-N	2PLAR-F
32	1C4 & 4PLR-E & F	6PLC-12

NOTE. THE PANEL SERVO-SUPPLY IS USED IN THE MODULATOR TUNING UNIT AND IN THE RECEIVER RADIO FREQUENCY. THE ANNOTATIONS COVER USE IN BOTH EQUIPMENTS. AND LEAD DESTINATIONS ARE GIVEN ABOVE IN TABLE 1

MOD RECORD
1 2 3 4 5 6
7 8 9 10 11 12

PANEL SERVO SUPPLY 5820-99-519-6986

SUB-ASSEMBLY 4 (REFERENCE PHASE & CONTROL CHOPPER) CIRCUIT DIAGRAM

FIG.17·3A

| | | |

| | | |

CHAPTER 18

PANEL RECEIVER AUXILIARY CIRCUITS

5820-99-519-7032

UNIT 6

CONTENTS LIST

	Paragraphs
Introduction	1 - 5
Physical Description	6
ELECTRICAL DESCRIPTION	7 - 16
Servo Supply Switch	7 - 13
A.F. Monitor	14
Ledex Protection Circuit	15 - 16

ILLUSTRATIONS

	Figure No
Panel Receiver Auxiliary Circuits Block Diagram	18.1
Panel Receiver Auxiliary Circuits Component Layout	18.2
Panel Receiver Auxiliary Circuits Circuit Diagram	18.3

CHAPTER 18

PANEL RECEIVER AUXILIARY CIRCUITS

5820-99-519-7032

UNIT 6

Introduction

Figure 18.1

1. The Panel Receiver Auxiliary Circuits contains three separate circuits, viz. a servo supply switch, a LOCAL/REMOTE 1/REMOTE 2 monitor stage, and a Ledex-protection circuit.

2. VT1 to VT7 and VT10, VT11, with their associated components, form the servo supply switch. It switches the -30 V supply to the 400 Hz oscillator and pre-amplifier and the -22 V supply to the reference and control amplifiers on Panel Servo Supply, unit 4 under the following conditions:

(a) When the Receiver is first switched on.

(b) When the servo is not in a null position.

(c) When the Synthesiser frequency is changed.

When the Synthesiser frequency is changed, the -30 V and -22 V supplies are applied until the servo motor runs to its correct position.

3. A delay in the servo supply switch maintains the -30 V and -22 V supplies for approximately 0.5 second after the final operation is completed, then switches them off.

4. Emitter-follower VT8 forms the Local/Remote 1/Remote 2 monitor stage, allowing one of the three line amplifiers to be monitored.

5. VT9 controls the Ledex protection circuit which interrupts the supply to the Ledex motor if it jams. The interruption is pulsed so that the motor current is insufficient to cause overheating while release of the jammed motor is encouraged.

Physical Description

6. Unit 6 is a plug-in printed wiring board 7.2 inches by 5.5 inches. A finger-pull facilitates removal and slotted guides assist location of the panel into its socket. Rubber pads on the printed-wiring side prevent it being inserted in the wrong position.

ELECTRICAL DESCRIPTION

Figure 18.3

Servo Supply Switch

7. VT1, VT2 form a Schmitt Trigger. The reference voltage at VT2 base is -25.4 V and is set by resistor network R3, R6, R7.

8. When the Receiver is functioning under normal signal conditions the -30 V and -22 V supplies are not applied to the Panel Servo Supply. VT2 is conducting and VT3 base is at approximately -25 V, VT4 is cut-off, VT5 is conducting and VT6, VT7, VT10, VT11 are cut-off.

9. While frequency is being changed or when the Receiver is first switched on, -30 V is applied to the servo 400 Hz oscillator and pre-amplifier and -22 V is applied to the reference and control amplifiers, allowing the servo mechanism to run towards a null position. Under this condition VT2 is non-conducting and VT3 base voltage is approximately -17.5 V. This is achieved by one of the following triggering methods:

(a) When the Receiver is first switched on a pulse is applied to VT1 base via C1, R1 due to the rapid rise of the -30 V supply. VT1 will conduct and VT2 will cut off so that VT3 base voltage is approximately -17.5 V.

(b) When the frequency is changed by operating one of the Frequency Synthesiser decade switches, the earth line is removed from VT1 collector via PLC10, thus cutting off VT2 and applying -30 V and -22 V to the Panel Servo Supply.

10. This condition is maintained until the servo has nulled. A d.c. voltage proportional to the servo output is applied to VT1 base via PLC8. In the off null condition the output of approximately -20 V maintains VT1 in a conducting condition. When a null position is reached this drops to approximately -26 V to -30 V which causes VT1 to cut off. VT2 conducts and removes the -30 V and -22 V supplies after a delay of approximately 0.5 second. The delay circuit C2, R12 allows the -30 V and -22 V supplies to the Panel Servo Supply to be maintained for approximately 0.5 second after the null has been reached, enabling the servo motor to reach a satisfactory null. After this delay the -30 V and -22 V supplies are switched off.

11. The -30 V and -22 V supplies to the Panel Servo Supply are also maintained if the Ledex is still in operation after the tuning servo has nulled. The -30 V supply for VT1, VT2 is made via MR1, MR2 to the range switches. VT2 is non-conducting while the Ledex is in an intermediate stage because there is no -30 V supply to its emitter, but when a range position is reached VT2 conducts. The -30 V and -22 V supplies to the Panel Servo Supply will be maintained, until the Ledex is on the correct range, by the action of the 0.5 second delay.

12. When VT2 is cut off, VT3 base is at -17.5 V and C2 is charged to approximately this potential. VT4, VT5 form a Schmitt trigger, the trigger level of which is approximately -25.5 V. Therefore, VT5 is cut off and VT6 base is at approximately -15 V. VT7 is bottomed, giving an output of a nominal -30 V to the Panel Servo Supply. VT10 is conducting, VT11 is bottomed giving an output of -22 V to the Panel Servo Supply.

13. When VT2 is switched into its conducting state, VT3 base is at a low potential and C2 discharges towards this potential via R12, VT4. When VT4 base reaches the potential of this second trigger, VT5 conducts. The time required for C2 to discharge from full charge to the triggering level is approximately 0.5 second. VT6 base is at approximately -25 V but Zener diode D1, a 6.8 V device, causes VT7 to cut-off, removing the -30 V supply from the Panel Servo Supply.

A.F. Monitor

14. This comprises emitter follower VT8 and associated circuitry. The input to VT8 is from the slider of RV2B, the VOLUME control on the front panel. VT8 provides a low impedance drive via C5, R25, to 1JKC and 1SKTAX, the H/SETS monitoring sockets on the front panel. The stage monitors any one of the three line amplifiers.

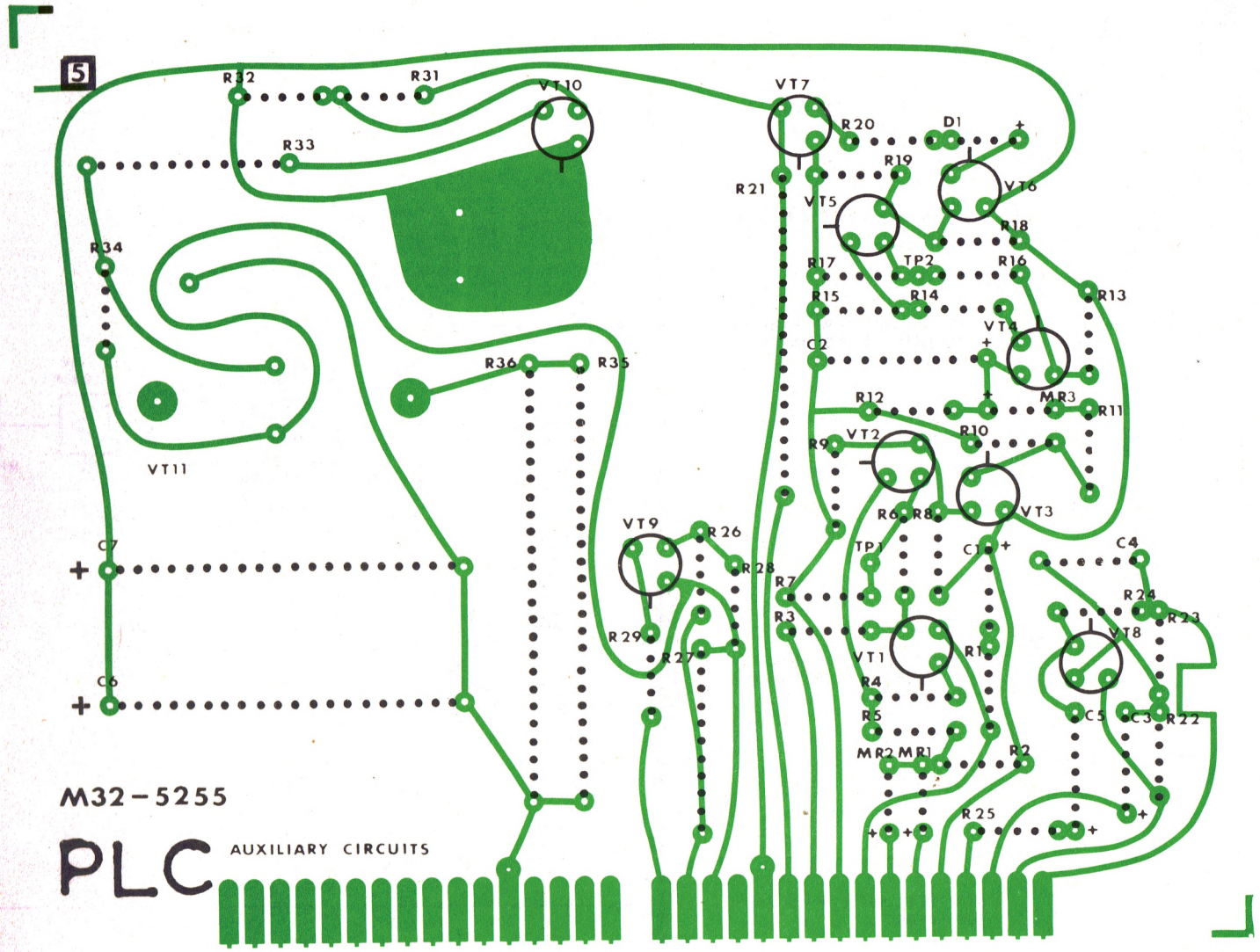
Ledex Protection Circuit

15. The Ledex motor is connected between the +41 V and -41 V unstabilised supply. The supply is fed via relay contact 1RLB1 which is normally made when 1RLB is de-energised. While the Ledex motor is running current is flowing through R27 and

a voltage is produced across it causing VT9 to conduct. Depending on the time constant of VT9 collector circuit and the period during which the Ledex motor takes current, 1RLB is energised or de-energised. If the Ledex motor jams 1RLB is energised, 1RLB1 breaks and the motor supply is disconnected. VT9 is cut-off and 1C2 starts to charge via 1RLB coil. The current in the relay coil falls exponentially and eventually the relay is de-energised, restoring the supply to the Ledex motor. This cycle is repeated until the Ledex motor is no longer jammed, or until the supply is switched off.

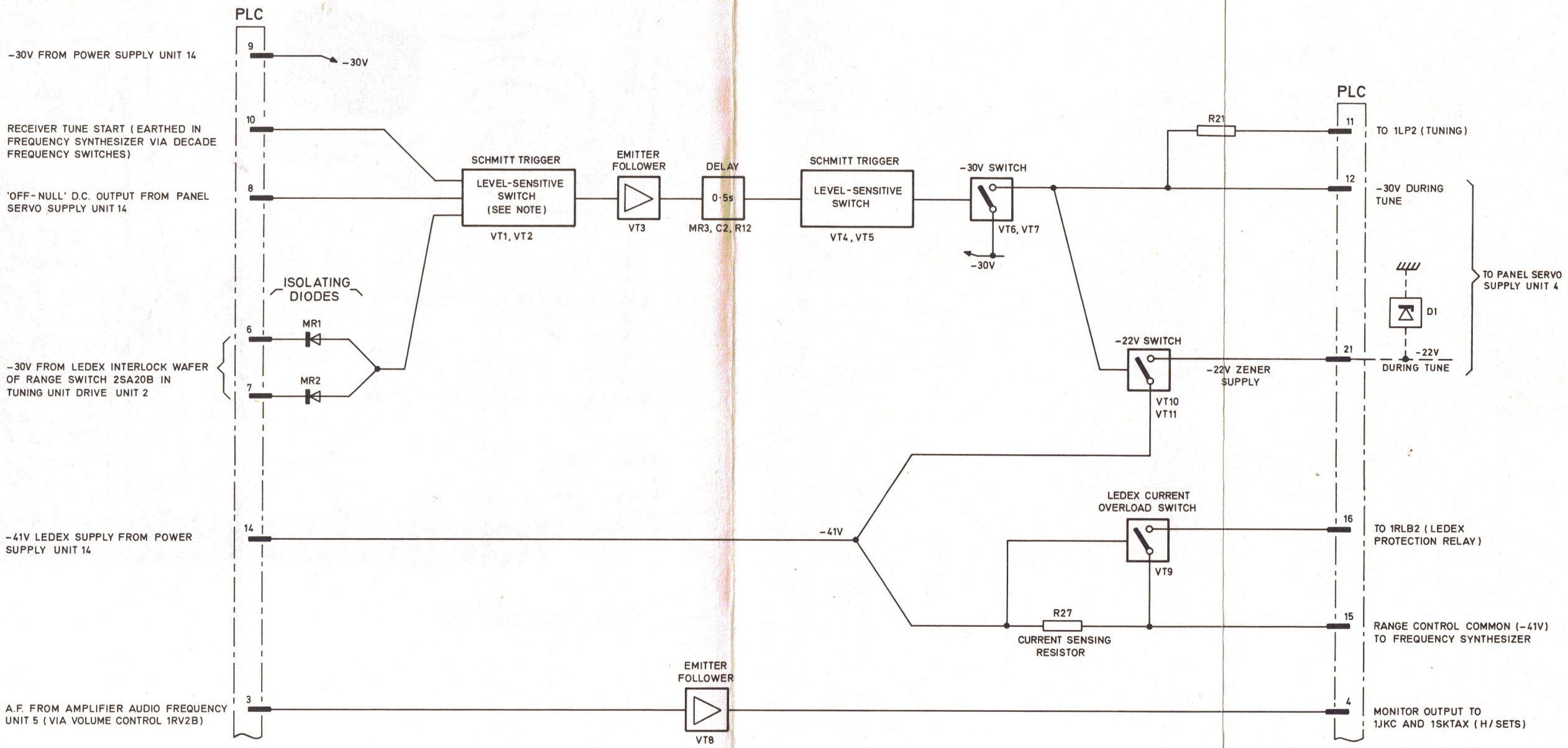
16. Relay contact 1RLB2 is in series with the CUTOUT lamp 1LP3 and gives the following indications:-

Ledex supply failure	-	Lamp on
Aerial overload	-	Lamp on
Ledex jammed	-	Lamp flashing.



M32-5255 L ISS 5

FIG. 18.2 PANEL RECEIVER AUXILIARY CIRCUITS COMPONENT LAYOUT



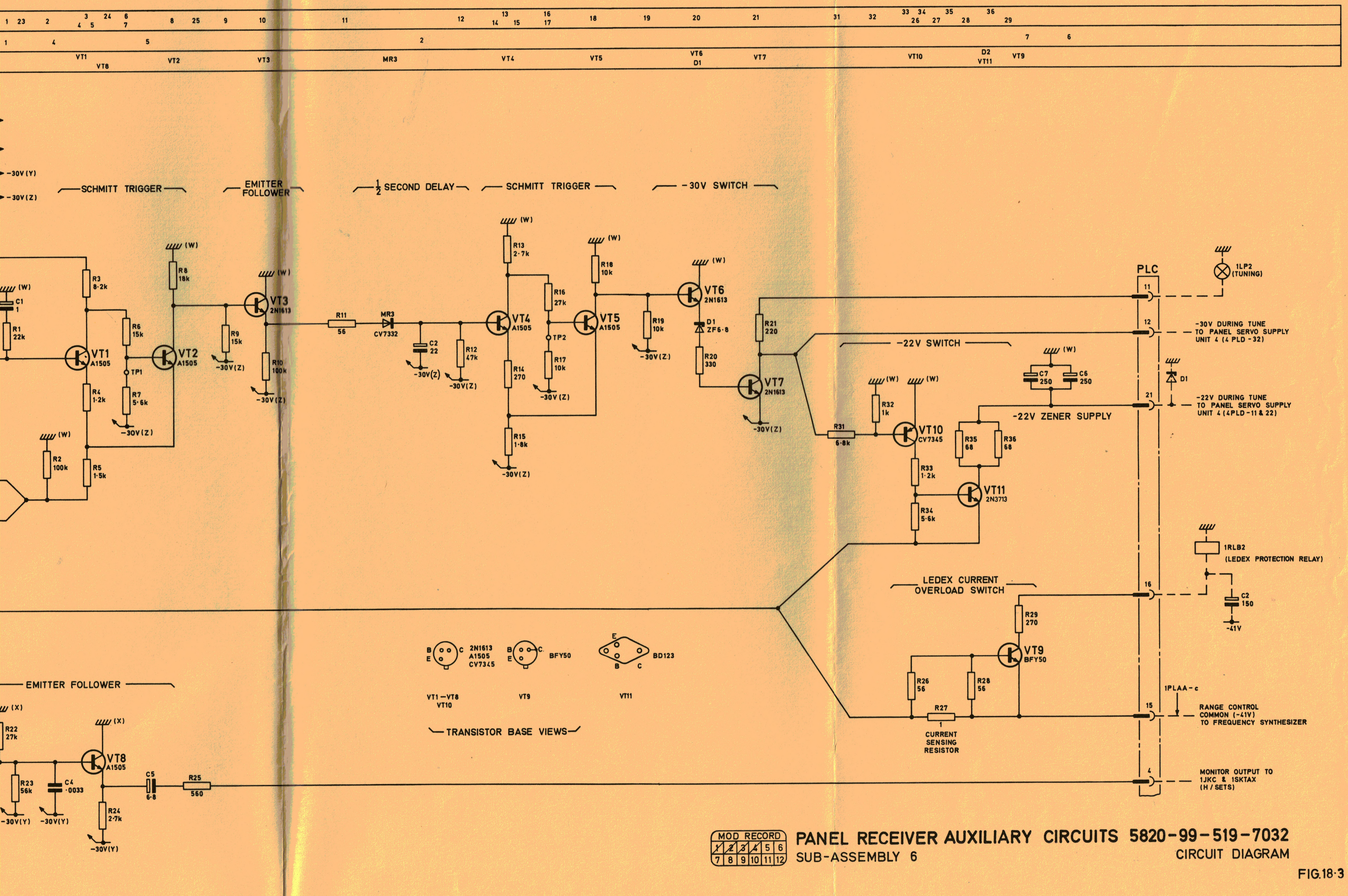
NOTE. OPERATION OF ANY SYNTHESIZER FREQUENCY SWITCH MOMENTARILY OPEN-CIRCUITS PLC-10, CLOSES -30V & -22V SWITCHES AND ENERGIZES TUNE SERVO SYSTEM. 'OFF-NULL' D.C. OUTPUT OF SERVO-AMPLIFIER HOLDS VT1 & VT2 IN THIS STATE UNTIL SERVO HAS NULLED AND $\frac{1}{2}$ SECOND DELAY HAS ELAPSED, AFTER WHICH THE -30V & -22V SWITCHES OPEN AND DE-ENERGIZE THE SERVO SYSTEM. LEDEX INTERLOCK OPEN-CIRCUITS PLC-6 & 7 IF RANGE SWITCH IS ROTATING BETWEEN POSITIONS AND ENSURES THAT -30V & -22V SWITCHES REMAIN CLOSED UNTIL AT LEAST $\frac{1}{2}$ SECOND AFTER RANGE SWITCH STOPS AT A POSITION.

PANEL RECEIVER AUXILIARY CIRCUITS 5820-99-519-7032

SUB ASSEMBLY 6

BLOCK DIAGRAM

FIG.18·1



MOD RECORD

1	2	3	4	5	6
7	8	9	10	11	12

PANEL RECEIVER AUXILIARY CIRCUITS 5820-99-519-7032

SUB-ASSEMBLY 6

CIRCUIT DIAGRAM

FIG. 18·3

| | | |

CHAPTER 19

POWER SUPPLY 5820-99-519-7022

UNIT 14

CONTENTS LIST

	Paragraphs
Introduction	1, 2
Physical Description	3 - 5
ELECTRICAL DESCRIPTION	6 - 25
+200 V h.t.	7
6.3 V a.c.	8
+70 V stabilised	9
+41 V and -41 V unstabilised	10
+30 V and -30 V stabilised	11
Stabiliser Boards Voltage Regulation	15 - 18
Stabiliser Boards Overload Protection	19 - 25

ILLUSTRATIONS

	Figure No
Basic Regulator	19.1
Regulator Differential Amplifier	19.2
Overload Protection Circuit	19.3
Power Supply Block Diagram	19.4
Stabiliser Board (+30 V) Unit 15 Component Layout	19.5
Stabiliser Board (-30 V) Unit 16 Component Layout	19.6
Component Board 5820-99-521-9423 Component Layout	19.7
Power Supply Component Layout	19.8
Power Supply Circuit Diagram	19.9

CHAPTER 19

POWER SUPPLY 5820-99-519-7022

UNIT 14

Introduction

1. The Power Supply provides the Receiver power supplies:

(a) +200 V d.c., 35 mA, stabilised for valve h.t.

(b) 6.3 V a.c., 1.5 A for valve heaters and indicating lamps.

(c) +41 V d.c., 3 A, unstabilised for Ledex motor.

(d) -41 V d.c., 3 A, unstabilised for Ledex motor and, via unit 6, for servo motor.

(e) +30 V d.c., 600 mA, stabilised for transistors, metering and audio output transformer.

(f) -30 V d.c., 600 mA, stabilised for transistors, diode switching and TUNE supply.

(g) +70 V d.c., stabilised for 100 kHz Oscillator varactor.

2. The mains transformer T1 has two primary windings, for series or parallel connection according to the mains voltage, and three secondary windings. All connections to the unit are made via 36-way plug PLAV. The SUPPLY ON/OFF switch 1SG on the front panel switches both line and neutral. The +200 V d.c. supply is protected by the HT+ fuse mounted on the front panel.

Physical Description

Figure 19.8

3. Unit 14 is a box-like chassis with a hinged panel on the underside that can be swung down after two screws have been removed. It is 6 inches high by 7.5 inches wide by 5 inches deep and it is secured by four captive screws.

4. On the top are inductor L1, transformer T1, and four preset potentiometers on a bracket. The hinged panel underneath carries six electrolytic capacitors C4-C9 and allows access to Component Board 5820-99-521-9423 and the terminals of T1.

5. Stabiliser Boards, units 15 and 16, are included in unit 14. They are plug-in printed wiring boards, polarised so that they cannot be fitted in the wrong socket and retained by a clamp plate. They must not be replaced with power ON. For heat dissipation their control transistors VT2, VT3 are mounted, with heat sinks, on the cabinet.

ELECTRICAL DESCRIPTION

Figures 19.4, 19.9

6. R1, C1, R2, C2 provide protection for the secondary circuits of T1 against transient voltage surges.

7. +200 V h.t. This supply for the r.f. amplifying valves 2V1, 2V2 is derived from the 180 V secondary of T1. Bridge rectifier MR1 to MR4 produces +230 V, smoothed by L1, C3. Zener diode D3 is then used in conjunction with R15, R16 to drop the unstabilised +230 V by 30 V and produce a stabilised +200 V output. A monitoring voltage is tapped from R15, R16 junction via R17 to the SUPPLIES, +230 V position of the front panel METERING switch 1M1.

8. 6.3 V a.c. Provided by the 6.3 V secondary of T1 to supply 2V1, 2V2 heaters. It also supplies indicator lamps as follows:

(a) 1LP1 via 1SG for SUPPLY, ON.

(b) 1LP3 via 1RLB2 for CUTOUT.

(c) 1LP8 via 1SD1F for RECEIVE USB/DSB.

(d) 1LP9 via 1SD1F and 1SF1B for RECEIVE LSB.

9. +70 V stabilised. This supply is obtained from the +230 V supply via dropping resistor R4 and Zener diodes D1, D2 which are returned to the +30 V supply. The two 20 V diodes in series hold the supply rail at 40 V above the 30 V supply, thus maintaining a stabilised 70 V supply.

10. +41 V and -41 V unstabilised. The 32-0-32 V secondary of T1 supplies a full-wave rectifier MR5 to MR8, which provides outputs of +41 V and -41 V, smoothed by C4 to C9, for the Ledex motor. The supply to the servo motor is fed via the Panel Auxiliary Circuits and from there controlled to provide -22 V.

11. +30 V and -30 V stabilised. Derived from +41 V and -41 V unstabilised, these supplies for transistor circuits are stabilised by Stabiliser Boards, Units 15 and 16. R11, R12 and R13, R14 provide monitoring voltages to the SUPPLIES +30 V and -30 V positions of the front panel METERING switch.

12. To cater for low mains conditions on full load, each Stabiliser Board includes a differential amplifier which requires a 48 V supply. In Unit 15 the +48 V zener supply is obtained from the +70 V zener supply via 14R6, 15PLA-16, 15R16, 15MR2, 15R1. The bridge rectifier 15MR1 to 15MR4 is used only when Unit 15 is used in a Modulator Tuning Unit. In Unit 16 the -48 V zener supply is obtained from the 32-0-32 V secondary of 14T1 via a voltage doubler 14R7, 14C10, 14MR9, 14MR10, 14C11 which provides -70 at 16PLB-16.

13. Four variable resistors allow adjustments to be made to the outputs of the two stabiliser boards. RV3 for the +30 V Stabiliser Board, Unit 15 and RV4 for the -30 V Stabiliser Board, Unit 16, set the outputs precisely. RV1 for unit 15 and RV2 for unit 16 set the current level at which the stabiliser protection circuits operate. The voltage operating the trip is developed across 14R8, 14R9. If the load current of either board exceeds 1.5 A the trip operates and clamps the output voltage to zero. The circuit may be restored by switching off the supply, waiting for approximately 30 seconds and then switching on again. Should the overload still be present, the trip will continue to operate.

14. VT2, VT3 are part of the stabiliser circuits, but for dissipation of heat they are mounted on heat sinks on the cabinet.

Stabiliser Boards Voltage Regulation — Figures 19.1, 19.2, 19.9

15. Figure 19.1 shows a series regulator, which is basically an emitter follower. If the voltage at the base is kept constant at Vo then the output voltage across RL is constant at Vo', which is approximately equal to Vo. This is so irrespective of Vs and RL, provided that Vs is greater than Vo.

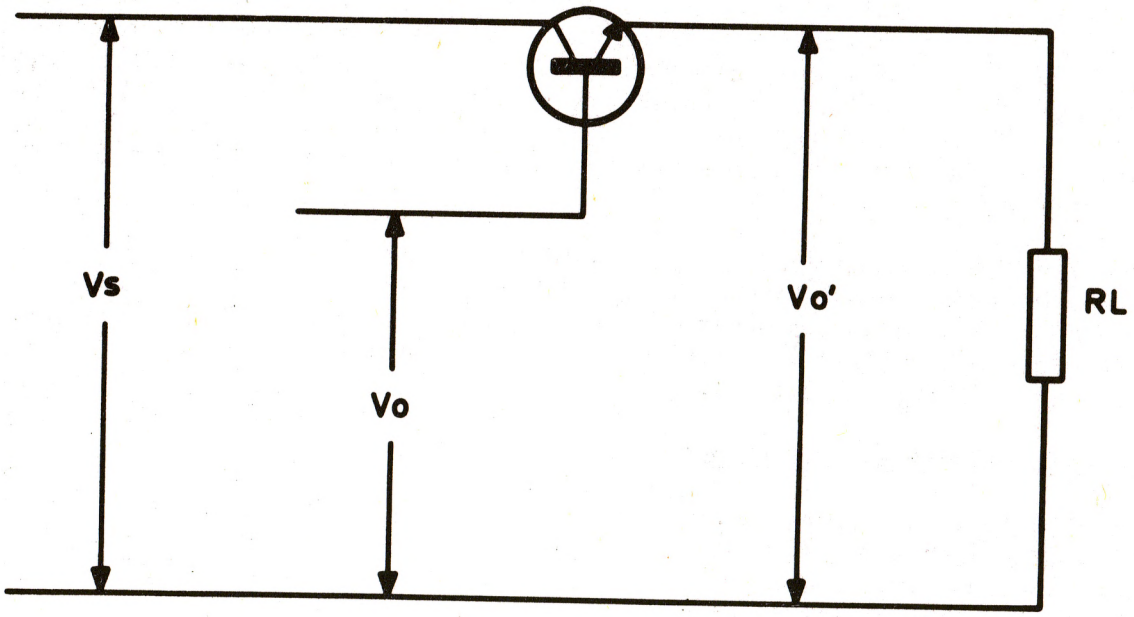


Fig 19.1 BASIC REGULATOR

16. Fig 19.2 shows an elaboration of the circuit, in which Vo is derived from a differential amplifier which compares a fraction of the output voltage with a precise reference voltage. This arrangement provides negative feedback, and any change in Vo' relative to the reference voltage produces a compensating change in Vo.

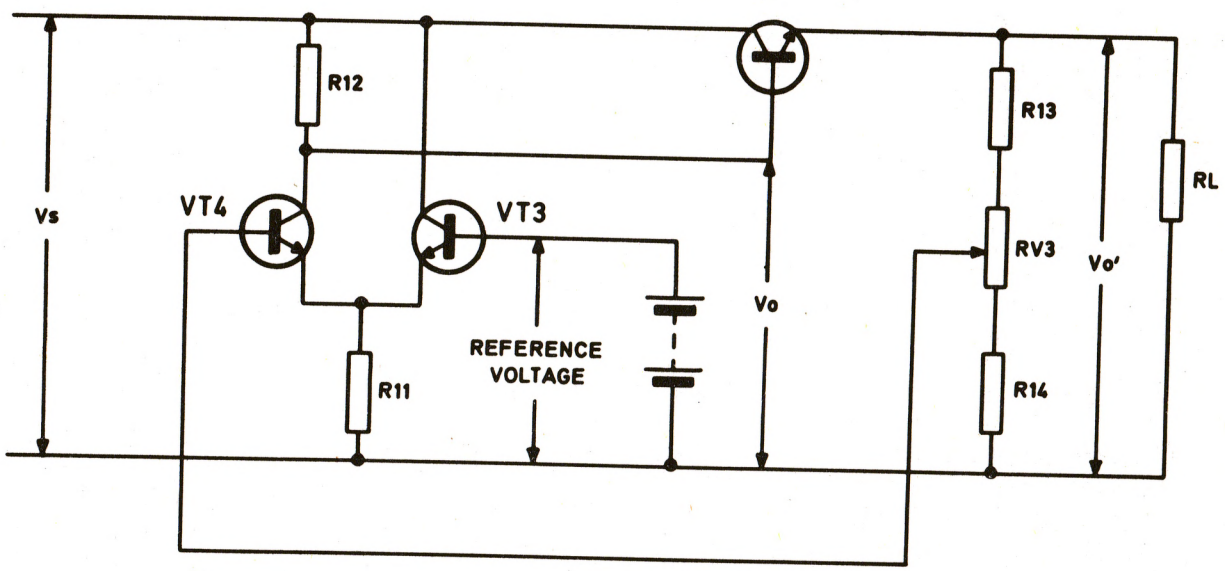


Fig 19.2 DIFFERENTIAL AMPLIFIER

17. In practive, on both Stabiliser Boards, the emitter follower comprises VT5, VT6 and the external power transistor VT2 or VT3. The reference voltage is obtained across Zener diode D4 or D2 which is energised from the output voltage via R10. VT3, VT4 with common emitter resistor R11 and load resistor R12 form the differential amplifier. The reference voltage is applied to VT3 base, and a proportion of the output to VT4 base, via set volts potentiometer 14RV3 or 14RV4. Because of the symmetry of the amplifier its gain is extremely stable with regard to temperature changes, variations in the emitter sensitivity of the two transistors being mutually compensating.

18. When the unstabilised $\pm$ 41 V input is low due to low mains input, it approaches the control voltage required at VT5 base and at VT4 collector. To ensure that regulation is unimpaired in this region of operation, the load R12 of the differential amplifier is returned to a supply line approximately 18 V higher than the voltage required at VT4 collector.

Stabiliser Boards Overload Protection — Figures 19.3, 19.9

19. VT1, VT2 form an overload protection circuit which, should the load current exceed the safe limit for the power transistors, will clamp the output voltage to near zero. Figure 19.3 shows the circuit, which is common to both boards. However, voltage changes in unit 15 are of opposite polarity to those in unit 16.

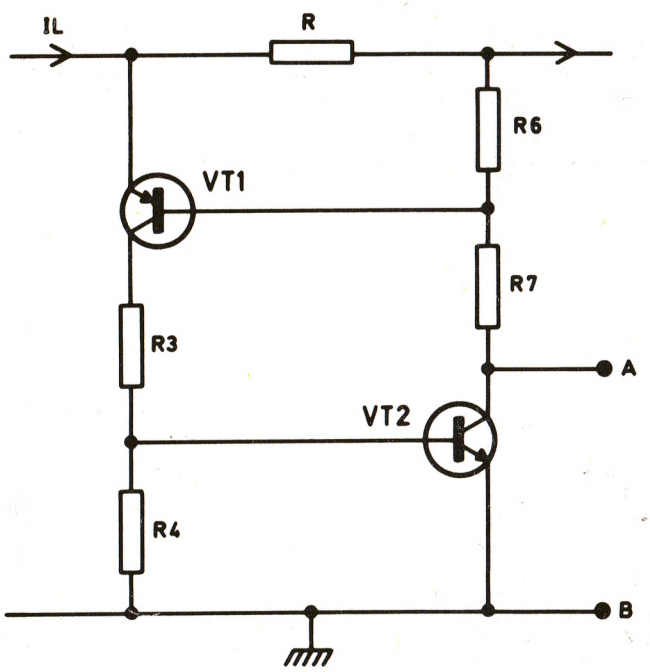


Fig 19.3 OVERLOAD PROTECTION CIRCUIT

20. The two transistors form a trigger circuit. When IL is zero VT1 base and emitter are at the same potential and VT1, VT2 are non-conducting. This state is maintained as IL increases, until the voltage developed across R is approximately 0.5 V, the inherent hold-off voltage of a silicon transistor. When IL increases further VT1 base becomes more negative with respect to its emitter, VT1 conducts and the voltage across R4 switches VT2 into conduction. This produces a voltage across R6 which is coupled to VT1 base so that the circuit action is regenerative. Thus a clamped state is reached, with both transistors conducting. Points A and B are then near short circuit.

21. In the Power Supply R is 1 ohm and is 14R8 for unit 15, 14R9 for unit 16. R2, R5, TH1 and the SET O/L potentiometer 14RV1 or 14RV2 form a potentiometer network allowing a proportion of the voltage developed across the 1 ohm resistor to be applied to VT1 base/emitter circuit. TH1 compensates for variations of VT1 hold-off voltage caused by temperature variations. When the load current is sufficient to trigger the circuit, the collector/emitter circuit of VT2 becomes a virtual short circuit, and VT5 base is tied to the common negative rail via 15MR7 or 16MR2, and VT2. The output is thus reduced to zero.

22. Once the trigger circuit has operated it will remain in that state even if the load is reduced. To reset it, it is necessary to switch off the mains supply to T1, and wait for about 30 seconds for capacitors C4 to C9 to discharge. The mains supply may then be switched on. If the overload fault persists the trip circuit will operate again.

23. 15C2 or 16C4 prevents the trip operating on short-duration high-current pulses, which may be greater than the trip current but within the pulse handling capability of the regulator transistor.

24. 15MR7 or 16MR2 prevents the trip circuit being triggered by a pulse at VT5 base. Normally, 15R8 or 16R9 holds VT2 collector at +44 V with respect to the negative line, so that 15MR7 or 16MR2 is back biased by approximately 13 V, thus breaking the circuit.

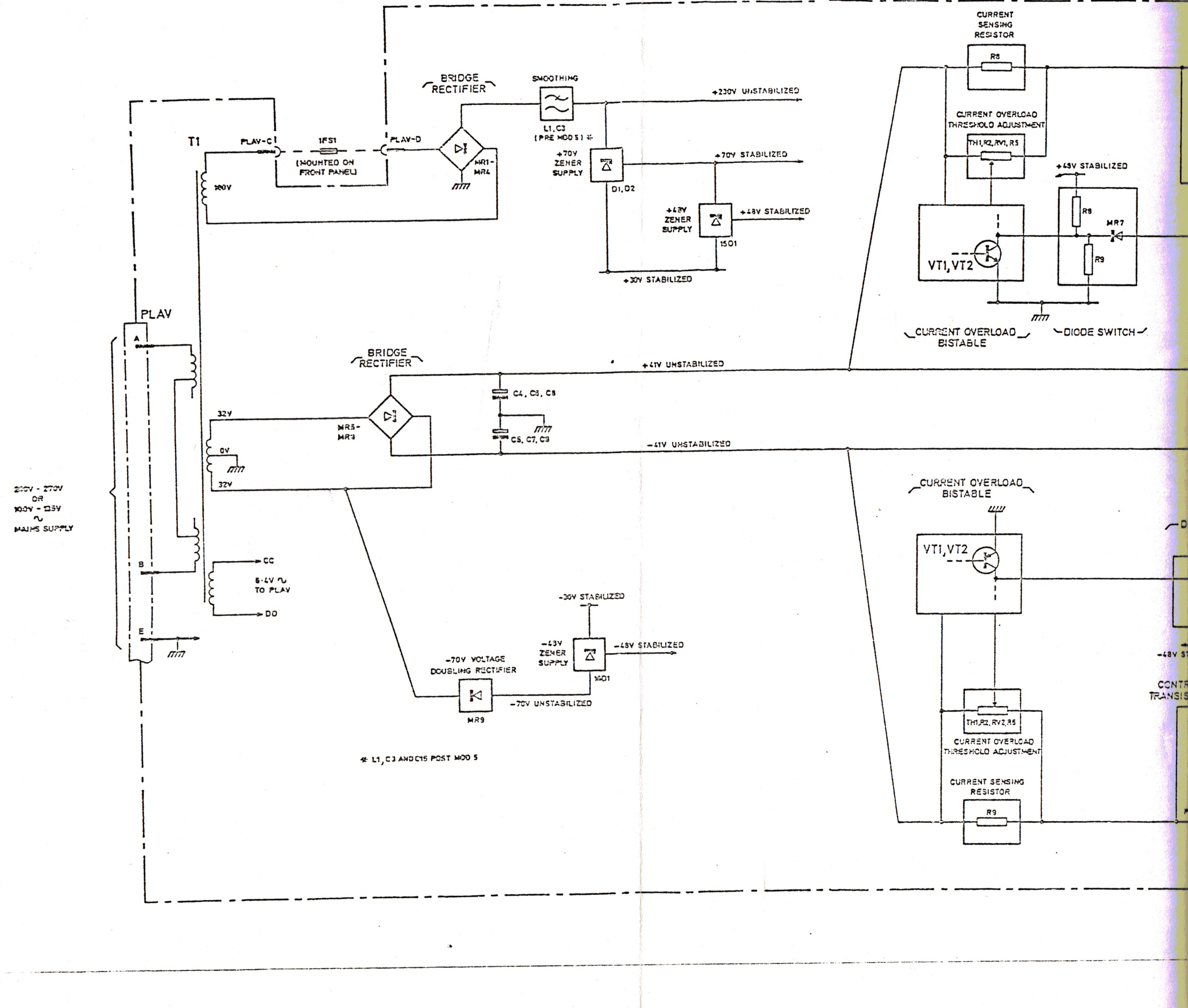
25. 15D2 prevents the collector/emitter rating of VT2 being exceeded under a high mains, no load condition. This is not required on unit 16 as 16VT2 has a higher collector/emitter rating. MR3, on unit 16 only, protects VT5 and VT6 against excessive reverse emitter/base voltage.

SMOOTHING
L1, C3
(PRE MOD 5) ✲
+230V UNSTABILIZED
+70V ZENER SUPPLY
D1, D2
+70V STABILIZED
+43V ZENER SUPPLY
1S01
+48V STABILIZED
+30V STABILIZED
+41V UNSTABILIZED
CURRENT SENSING RESISTOR
R8
CURRENT OVERLOAD THRESHOLD ADJUSTMENT
TH1, R2, RV1, R5
+43V STABILIZED
R8
MR7
R9
VT1, VT2
CURRENT OVERLOAD BISTABLE
DIODE SWITCH
PLAV-H
SERIES REGULATOR
+30V STABILIZED OUTPUT
VT2
(MOUNTED ON CABINET)
PLAV-H
PLAV-S
VT5, VT6
CONTROL TRANSISTORS
+43V STABILIZED
R3
R4
RV3
DIFFERENTIAL AMPLIFIER
VT3, VT4
D4
SET OUTPUT VOLTS
ZENER REFERENCE
+230V UNSTABILIZED
1403
30V
R15
R17
R16
R11
R12
R15
+70V STABILIZED
METER MULTIPLIER RESISTOR CHAINS
PLAV
F
T
U
V
P
BB
X
N
AA
+200V H.T. TO TUNING UNIT RECEIVER UNIT 2
+200V H.T. TO VLF ADAPTOR (WHEN FITTED)
METERING (SUPPLIES +230V)
METERING (SUPPLIES +30V)
TO 1M1
+70V STABILIZED TO FINE TUNING CIRCUIT (1RV4 & 1SA1F)
+41V UNSTABILIZED LEDEX SUPPLY
EARTH TO VLF ADAPTOR (WHEN FITTED)
EARTH TO TUNING UNIT RECEIVER UNIT 2
+41V UNSTABILIZED LEDEX SUPPLY
W
METERING TO 1M1 (SUPPLIES -30V)
CC
DD
6.4V ~ FROM T1
HEATER SUPPLY TO VLF ADAPTOR WHEN FITTED

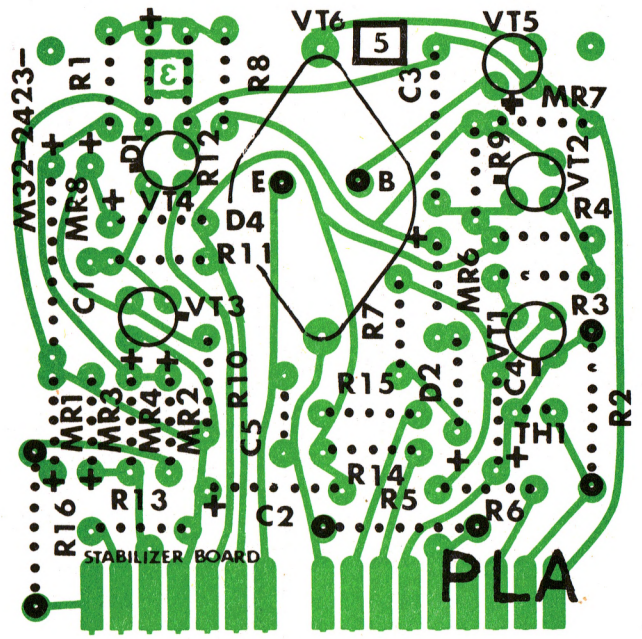
-41V UNSTABILIZED
-30V STABILIZED
-43V ZENER SUPPLY
1S01
-48V STABILIZED
UNSTABILIZED
CURRENT OVERLOAD BISTABLE
VT1, VT2
TH1, R2, RV2, R5
CURRENT OVERLOAD THRESHOLD ADJUSTMENT
CURRENT SENSING RESISTOR
R9
DIODE SWITCH
MR2
MR3
-48V STABILIZED
CONTROL TRANSISTORS
VT5, VT6
PLAV-R
PLAV-L
VT3
(MOUNTED ON CABINET)
SERIES REGULATOR
-30V STABILIZED OUTPUT
SET OUTPUT VOLTS
R3
R4
RV4
DIFFERENTIAL AMPLIFIER
VT3, VT4
D2
ZENER REFERENCE
-48V STABILIZED
METER MULTIPLIER
R13
R14
R15
PLAV-Y

POWER SUPPLY 5820-99-519-7022
SUB-ASSEMBLY 14 BLOCK DIAGRAM

FIG. 19-4

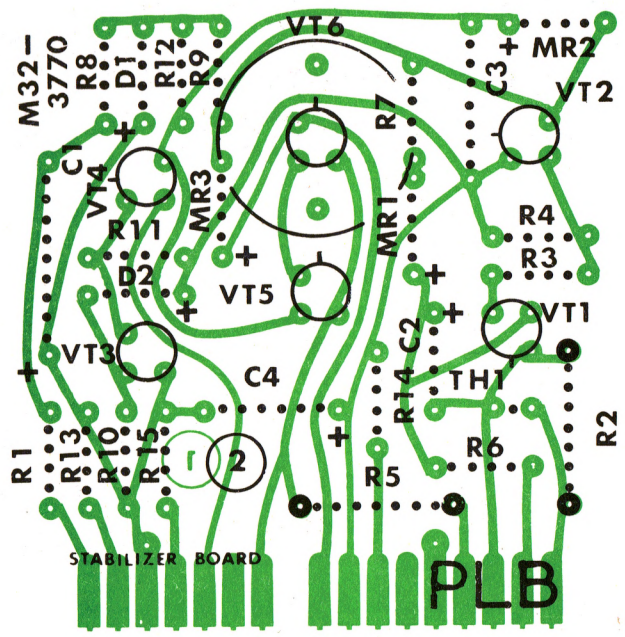


* L1, C3 AND C15 POST MOD 5



M32-2423 L ISS 5

STABILISER BOARD (+30V) UNIT 15 COMPONENT LAYOUT FIG. 19.5



M32 3770(L) ISS 2

STABILISER BOARD (-30V) UNIT 16 COMPONENT LAYOUT FIG. 19.6

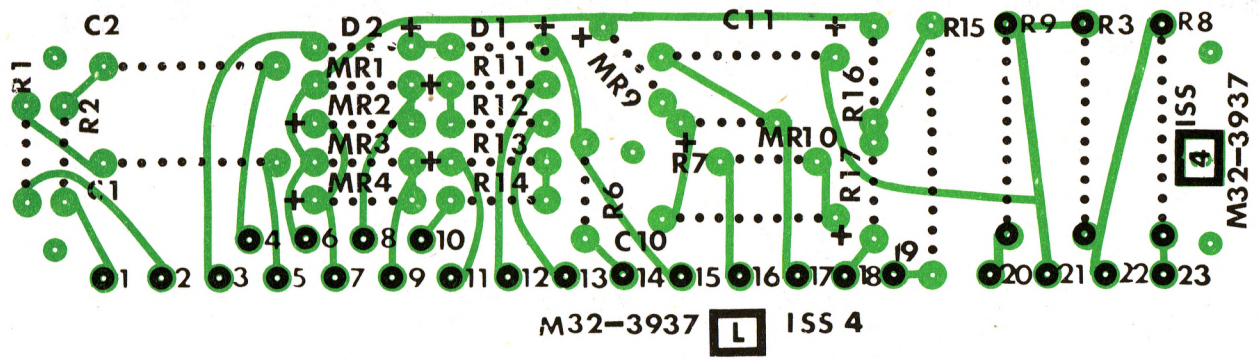
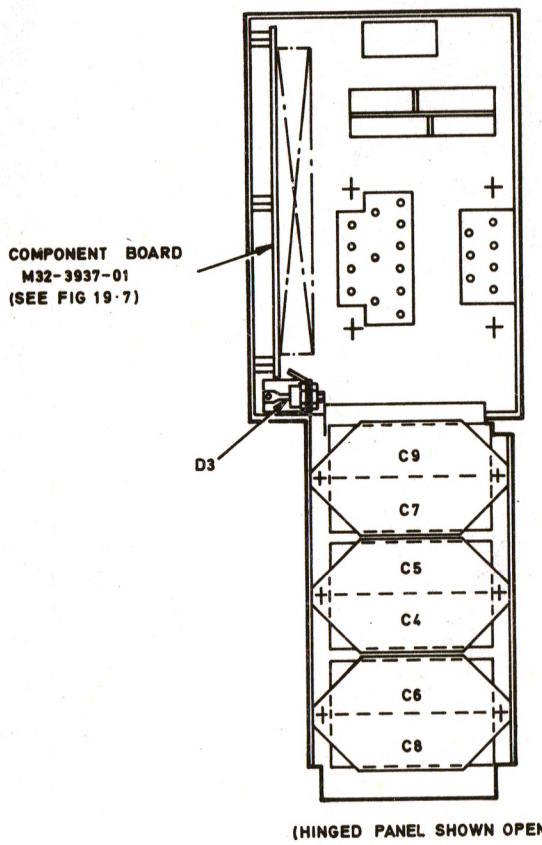
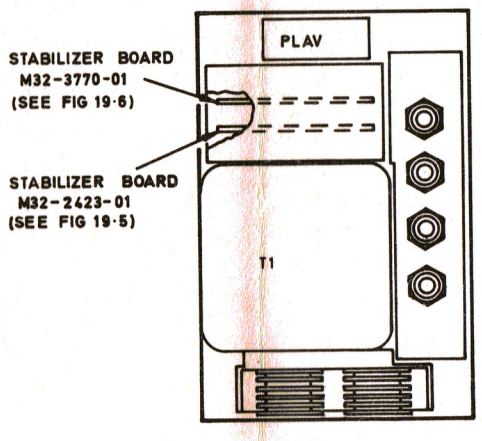
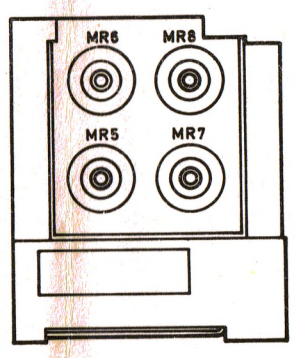


FIG. 19.7 COMPONENT BOARD COMPONENT LAYOUT

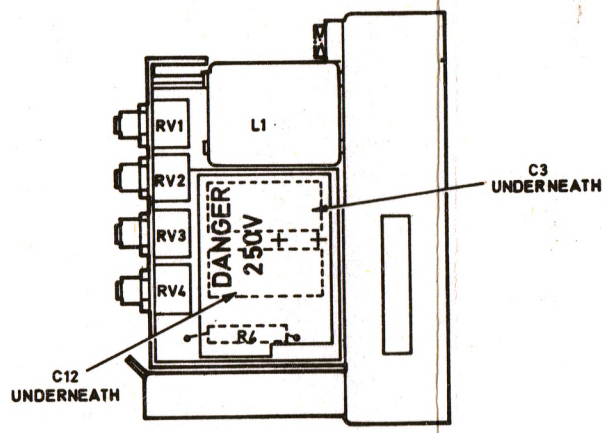


(HINGED PANEL SHOWN OPEN)





POWER SUPPLY M32-2901-01
(N.S.N. 5820-99-519-7022)



POWER SUPPLY **5820-99-519-7022**

INCLUDING STABILIZING BOARD SUB-ASSEMBLY 15 5820-99-521-9421
STABILIZING BOARD SUB-ASSEMBLY 16 5820-99-521-9422
COMPONENT BOARD 5820-99-521-9423
SUB-ASSEMBLY 14 COMPONENT LAYOUT

FIG. 19·8

BASE VIEWS

ISV15 ISV11 — BFY50 B C E

ISV16 ISV12 ISV14 ISV13 — BD123 B C E; AC125 CV7345 B C E

CABINET

PART OF

TS2 25 — ISG OFF ON — IPLAA Z — PLAV A

TILP6 TILP5

FS3 1A — R1 220R — R2 220R

R3 56k — R2 56k — TIPLZ

T1 — 240V — 180V — 150V — 120V — 100V — 70V — 34V — 32V — 6V — 0V

PART OF COMPONENT BOARD (5820-99-521-9423)

R2 2.7k — C2 .047 — R1 2.7k — C1 .047

MOUNTED ON FRONT PANEL — TILP5 FS1 1A — IR6

PART OF STABILIZER BOARD (5820-99-521-9422)

PART OF COMPONENT BOARD (5820-99-521-9423)

PART OF STABILIZER BOARD (5820-99-521-9421)

-48V ZENER SUPPLY

-70V VOLTAGE DOUBLER

± 41V RECTIFIER AND SMOOTHING

+48V ZENER SUPPLY

+ 230V RECTIFIER AND SMOOTHING

POWER SUPPLY (5820-99-519-7022)

TO PLAV

TO D3

T1 BASE VIEW

CURRENT OVERLOAD

LEDEX PLAV-BB PLAV-AA SUPPLY +41V -41V

NOT CONNECTED

STABILIZED

FROM PLA-11

FROM PLAV-5

FROM PLAV-3

FROM PLB-16

BR 2147(5)A
Amdt 4, 12.78

+48V ZENER SUPPLY

PART OF STABILIZER BOARD (5820-99-521-9421) 15

R16 220 (5820-99-521-9421)

MR1 MR2 MR3 MR4 4X CV7332

C1 22

R1 1·5k

D1 ZFB18

+70V

+48V

+30V STABILIZED (FROM PLA-13)

CURRENT SENSING RESISTOR

PART OF COMPONENT BOARD (5820-99-521-9423)

R8

SERIES REGULATOR

VT2 MOUNTED ON CABINET

1PLAA-m 1PLAA-k 1TS1 1PLAV-j PLAV-M PLAV-S PLA-9 PLA-10 PLA-11

+30V STABILIZED (TO D2)

+30V STABILIZED OUTPUT

CURRENT OVERLOAD THRESHOLD ADJUSTMENT

TH1 VA1034 R2 12 SET O/L I RV1 25 R5 10

VT6 2N3713

VT5 BFY50

CONTROL TRANSISTORS

PLA-6 PLA-2 PLA-5

C4 2·2

VT1 GM3991*

PLA-3

R6 47

R7 2·2k

D2 CV7101 5·6V MR6 CV7332

DIODE SWITCH

+48V R8 10k MR7 CV7332

PART OF STABILIZER BOARD (5820-99-521-9421) 15

R3 4·7

VT2 A1505

R4 4·7k

R9 100k C3 ·04

PLA-11

CURRENT OVERLOAD BISTABLE

+30V STABILIZED (TO D1)

15

R13 4·7k

+48V R12 15k

R10 2·2k

PLA-15

SET +30V RV3 500

PLA-12

VT4 A1505

VT3 A1505

C2 4·7

MR8 CV7332

D4 CV7101

PLA-7

R14 1k

R11 1·8k

R15 100k

PLA-8

SET OUTPUT VOLTS

DIFFERENTIAL AMPLIFIER

ZENER REFERENCE

METER MULTIPLIER RESISTOR CHAINS

+23CV FROM L1

D3 CV7256 30V

PART OF COMPONENT BOARD (5820-99-521-9423)

R15 500k R17 390k R16 47k R12 10k R11 390k R15 100k

PLAV

2PLAQ-B +200V H.T. TO TUNING UNIT RECEIVER UNIT 2

1PLAA-B +200V H.T. TO V.L.F. ADAPTOR - WHEN FITTED

1SB1F-38 METERING TO 1M1 (SUPPLIES +230V)

1SB2F-33 METERING TO 1M1 SUPPLIES +30V

+70V (FROM D1)

1RV4 TO FINE TUNING CIRCUIT (1SA1F)

+41V (FROM MR6/MR8)

2PLAC-A 1PLAA-a +41V SUPPLY TO LEDEX

1RLB1 1RS 33 C1 2·2

1PLAA-E EARTH TO V.L.F. ADAPTOR WHEN FITTED

2PLAQ-F EARTH

-41V

6PLC-16 -41V TO LEDEX VIA PANEL AUXILIARY CIRCUIT UNIT 6

1SB2F-35 METERING TO 1M1 (SUPPLIES -30V)

13PL4 1FS2 2·5A 1PLAA-H 11LP1 SUPPLY 1PLAA-D

6·4V SUPPLY FROM T1

HEATER SUPPLY TO V.L.F. ADAPTOR WHEN FITTED

+41V PLAV-BB PLAV-AA -41V LEDEX SUPPLY

-8V ZENER SUPPLY

PART OF STABILIZER BOARD (5820-99-521-9422) 16

-30V STABILIZED

D1 ZF18 -48V R8 1·5k R1 8·2k C1 22

PLB-16

CURRENT OVERLOAD BISTABLE

DIODE SWITCH

PLB-8

R4 4·7

VT2 CV7345

C3 ·03

PART OF STABILIZER BOARD (5820-99-521-9422) 16

R3 4·7

MR1 CV7332 R7 2·2k R9 10k -48V

VT1 BFY50

C2 1

R6 47

PLB

MR2 CV7332 MR3 CV7332

CONTROL TRANSISTORS

VT5 CV7345

PLB-3 R2 18 PLB-1 RV2 25 SET O/L I PLB-4 R5 33

TH1 VA1034

VT6 BFX29

PLB-10 PLB-9

16

R12 1k R11 1·8k D2 CV7101 C4 4·7

PLB-7

SET -30V RV4 500

PLB-12

VT4 CV7345 VT3 CV7345

PLB-15

R12 15k R10 2·2k

R13 4·7k -48V

PLB-13

R14 10k R13 390k R15 100k

PLB-14

-30V STABILIZED

CURRENT OVERLOAD THRESHOLD ADJUSTMENT

CURRENT SENSING RESISTOR

PART OF COMPONENT BOARD (5820-99-521-9423)

R9

PLAV-R PLAV-V

1PLAA-f 1PLAA-d 1PLAA-h

PLAV-L 1TS2

1VT3 MOUNTED ON CABINET

SERIES REGULATOR

-30V STABILIZED OUTPUT

* AMEND 6 VT1 = CV7344

MOD RECORD

1	2	3	4	5	6
7	8	9	10	11	12

POWER SUPPLY 5820-99-519-7022

INCLUDING: COMPONENT BOARD 5820-99-521-9423

STABILIZING BOARDS (SUB-ASSY'S. 15/16) 5820-99-521-9421/9422

SUB-ASSEMBLY 14 CIRCUIT DIAGRAM

FIG.19

CHAPTER 20

MODIFICATIONS

CONTENTS LIST

	Paragraphs
Introduction	1
CHASSIS AND FRONT PANEL ASSEMBLY, UNIT 1	2 - 12
Modification No 1	2
Modification No 2	3
Modification No 3	4 - 8
Modification No 4	9
Modification No 5	10
Modification No 6	11
Modification No 7	12
TUNING UNIT RECEIVER, UNIT 2	13 - 19
Modification No 1	13
Modification No 2	14
Modification No 3	15
Modification No 4	16
Modification No 5	17
Modification No 6	18
Modification No 7	19
AMPLIFIER INTERMEDIATE FREQUENCY, UNITS 10, 11	20 - 21
Modification No 1	20
Modification No 2	21
FREQUENCY OFFSET UNIT, UNIT 3	22 - 23
Modification No 1	22
Modification No 2	23
TEST EXTENSION ELECTRONIC CIRCUIT PANEL, 32-WAY, M32-2933-01	24
Modification No 1	24
PANEL SERVO SUPPLY, UNIT 4	25 - 31
Modification No 1	25
Modification No 2	26
Modification No 3	27 - 30
Modification No 4	31
POWER SUPPLY, UNIT 14	32 - 34
Modification No 1	32
Modification No 2	33
Modification No 3	34
PANEL AUTOMATIC GAIN CONTROL, UNITS 8, 9	35
Modification No 1	35
PANEL DEMODULATOR, UNIT 7	36
Modification No 1	36

CONTENTS LIST (Cont'd)

	Paragraphs
PANEL RECEIVER AUXILIARY CIRCUITS, UNIT 6	37 - 40
Modification No 1	37
Modification No 2	38
Modification No 3	39
Modification No 4	40
PANEL FILTER SWITCHING, UNIT 12	41
Modification No 1	41
CABINET, R.F. RECEIVER 5820-99-519-7018	42 - 44
Modification No 1	42
Modification No 2	43
Modification No 3	44
AMPLIFIER AUDIO FREQUENCY, UNIT 5	45
Modification No 1	45
TEST EXTENSION ELECTRONIC CIRCUIT PANEL, 16-WAY, M32-5264-01	46

CHAPTER 20

MODIFICATIONS

Introduction

1. This chapter lists the modifications that have been made to the Receiver Radio Frequency to March 1971.

CHASSIS AND FRONT PANEL ASSEMBLY, UNIT 1

Modification No 1

2. Socket SKTD for Panel Servo Supply, unit 4. Cable No 9 transferred from terminal 24 to terminal 22 and a link added between terminals 9 and 24. Incorporated to reduce ripple on the -30 V line.

Modification No 2

3. R7 changed to 39 k and all resistors associated with switch SA1 changed. Connection RV3, C3 transferred to SA1 tag 11. Incorporated at the same time as Modification No 1 to Tuning Unit Receiver, unit 2, to improve performance.

Modification No 3

4. R7 removed from front panel. Resistors changed: R9 from 118 k to 22k, R10 from 220 k to 150 k, R12 from 56 k to 120 k, R14 from 68 k to 120 k, R16 from 82 k to 150 k, R20 from 68 k to 39 k, R22 from 12 k to 10 k, R24 from 15 k to 8.2 k, R26 from 33 k to 5.6 k.

5. Connections removed between SKTD9 and SKTAV-J, SKTD22 and SKTAV-K, SKTD11 and SKTD17, SKTD17 and SKTD12. Connections removed from SKTD11 and connected to SKTD10. New connections made from SKTD10 to SKTD17, SKTD21 to SKTD11, SKTD11 to SKTD22, SKTD1 to SKTD9.

6. 10 k resistor between PLEQ and PLER removed. New stand-off terminal fitted at PLEQ, PLER. New diode D1 fitted between PLER and new terminal. R1, 22 ohms, connected between solder tag under PLER and new terminal. R2, 15 k, fitted between new terminal and PLEQ.

7. Part (A) of this modification carried out in conjunction with Modification No 3 to Tuning Unit Receiver, unit 2. Part (B) carried out in conjunction with Modification No 2 to Power Supply, unit 14, Modification No 3 to Panel Servo Supply, unit 4, and Part (C) carried out in conjunction with Modification No 1, Part (A), to Panel Demodulator, unit 7.

8. Incorporated to correct the voltage law on the switch to correspond with the modified 100 kHz Oscillator Board; to allow the Panel Receiver Auxiliary Circuits to supply -22 V to the servo circuit; to improve switching of the 100 kHz injection to below noise level.

Modification No 4

9. Drill holes in the right hand side and fit zener diode D1. Incorporated at the same time as Modification No 7 to Tuning Unit Receiver, to provide an infinite heat sink for D1.

Modification No 5

10. R27, 180 k, removed from switch SA tags 11 and 22. Incorporated to provide correct varactor tracking law for the 100 kHz Oscillator Board used on the Tuning Unit Receiver for Modification No 7.

Modification No 6

11. Jack sockets JKA, JKB and JKC replaced by new sockets which accept "A" gauge jack plugs.

Modification No 7

12. Points behind the front panel insulated, to prevent short circuits.

TUNING UNIT RECEIVER, UNIT 2

Modification No 1

13. R24 changed from 3.9 k to 4.7 k. C24, selected on test, added. Incorporated at the same time as Modification No 2 to unit 1, to improve unit performance to specified limits.

Modification No 2

14. Trimming access hole made larger for, and a locknut added to each of the capacitors: C14, C24, C44, C54, C64 in the R.F. Amplifier Assembly and C15, C16, C25, C26, C35, C36, C45, C46, C55, C56, C65, C66, C101, C102, C201, C301, C302, C401, C501, C601, C602. Incorporated to improve capacitor locking.

Modification No 3

15(a) 100 kHz Oscillator Board, unit 22. C2, 0.047 µF removed C25 330 pF, added in parallel with R14. Resistors changed: R15 from 2.2 k to 4.7 k, R4 from 390 to 68, R24 from 4.7 k to 8.2 k, R25 from 470 to 180, R26 from 3.3 k to 5.6 k. MR2, MR3 changed from CV7332 to IN3065. VT4, VT5 changed from A1505 to BC107. Incorporated to improve overall performance.

(b) 1 MHz I.F. Board, unit 20. R19, 680 ohms changed to 1 k. Incorporated to reduce gain in the i.f. stage.

(c) First Frequency Changer Board, unit 21. Resistors changed: R28 from 82 to 56, R37 from 1.5 k to 150 ohms. Incorporated to reduce the injection levels.

Modification No 4

16. Capacitors changed: C83 to 0.001 µF, C97 to 0.001 µF. Incorporated to bring the nominal inductance required to the centre of the tuning range of the existing coil design.

Modification No 5

17. Inductor L21 replaced by a kit of parts (M32-5153 Sheet 1, Issue 4). C121, C122 removed. C110 changed to 10 pF. Incorporated to improve the performance of the unit for common aerial working and for high voltage off channel working.

Modification No 6

18. Couplings O/D P.C.25535/1 removed and replaced by O/D P.C.25512/1. Incorporated to ensure proper alignment of switches in the tuning unit.

Modification No 7

19. 100 kHz Oscillator Board, unit 22. Inductance L604 added between crystal lead and pin, with facility to short out if required. C25 removed. Board identity changed to M32-2509-02. Incorporated at the same time as Modification No 5 to unit 1, to give greater range of frequency pulling without loss of gain and to accommodate tolerance range of crystals and varactors used.

AMPLIFIER INTERMEDIATE FREQUENCY, UNITS 10, 11

Modification No 1

20. 47 pF capacitor connected to transformer T7 between pins 8 and 3. Incorporated to prevent spurious high frequencies.

Modification No 2

21. R8 changed to 180 ohms, R23 changed to 150 ohms. Incorporated at the same time as Modification No 1 to unit 6, Modification No 3 to unit 2, Modification No 1 to unit 7, Modification No 3 to unit 1, to reduce the gain in the 100 kHz circuitry.

FREQUENCY OFFSET UNIT, UNIT 3

Modification No 1

22. VT9 changed from A1505 to U3065, to improve high frequency response.

Modification No 2

23. Link connected from screen of L32 to RV10, to allow the First Frequency Changer level to be set as specified.

TEST EXTENSION ELECTRONIC CIRCUIT PANEL, 32-WAY, M32-2933-01

Modification No 1

24. Test extension panel M32-2933-01, drawing issue 4 changed for new extension panel M32-2933-01, drawing issue 5, to make printed boards more accessible during tests.

PANEL SERVO SUPPLY, UNIT 4

Modification No 1

25. Transformer T1 redesigned, changed from M32-2527-01 to M32-2527-02. Incorporated to prevent protruding copper foil short circuiting to earth.

Modification No 2

26. R17, R18, R50, R52 changed from 33 k to 47 k. Incorporated to prevent overdissipation of output transistors when voltage rises to nearly 30 V in the "off-tune" condition.

Modification No 3

27. Resistors changed: R8 to 2.7 k, R9 to 1 k, R13 to 22 k, R14 to 560, R15 to 1 k, R17 to 33 k, R18 to 33 k, R26 to 47 k, R27 to 47 k, R28 to 2.2 m, R32 to 120 k, R34 to 180 k, R38 to 680, R39 to 6.8 k, R41 to 270, R42 to 10 k, R44 to 180, R45 to 18 k, R47 to 22 k, R48 to 560, R49 to 1 k, R50 to 33 k, R52 to 33 k.

28. Capacitors changed: C5 to 0.22 µF, C19 to 0.22 µF, C21 to 0.068 µF, C26 to 0.22 µF, C13 to 0.22 µF, C14 to 0.22 µF.

29. 560 ohm resistors R64, R65 added. Capacitors C18, C24, C37 removed. Transistor VT9 changed to type BC109. Printed board track altered and legend changed.

30. Incorporated at the same time as Modification No 3 Part B to Unit 1, Modification No 2 to Unit 2, Modification No 1 to Unit 6, to prevent overloading the amplifiers and to improve performance.

Modification No 4

31. R6 removed. R9 changed to 1.2 k. C17 changed to 6.8 µF. Incorporated to ensure satisfactory completion of tuning and prevent tendency for TUNE lamp to stay on.

POWER SUPPLY, UNIT 14

Modification No 1

32. 500 µF capacitor C12 connected between R18, R19 and PLAV-K. Incorporated at the same time as Modification No 1 to Unit 1, to reduce ripple on the -30 V line caused by the servo circuit operation.

Modification No 2

33. R18, R19, C12, associated wires and sleeves removed. Incorporated in conjunction with Modification No 3 Part B to Unit 1, Modification No 3 to Unit 4, Modification No 1 to Unit 6. Components no longer required.

Modification No 3

34. 1 µF capacitor C13 connected across 6.4 V winding of T1. Incorporated to prevent noise spikes, produced in 30 V rectifier circuits, from being transmitted via 6.3 V heater line to the Tuning Unit and affecting the signal to noise performance of the Receiver on the MF band.

PANEL AUTOMATIC GAIN CONTROL, UNITS 8, 9

Modification No 1

35. R64 connected from negative end of D3 and R60. R65 connected from R60 and existing earth. Incorporated to ensure satisfactory release of the signal relay which now requires a higher operate/release voltage ratio.

PANEL DEMODULATOR, UNIT 7

Modification No 1

36(a) C54 removed and replaced by a wire link. Incorporated at the same time as Modification No 3 Part C to Unit 1, to facilitate switching of 13D1 on the Crystal Filter Assembly.

(b) Remove screen from Panel Receiver Auxiliary Circuits, Unit 6, cut off joggle and replace screen. Incorporated at the same time as Modification No 1 to Unit 6, to facilitate removal of Unit 6.

PANEL RECEIVER AUXILIARY CIRCUITS, UNIT 6

Modification No 1

37. Resistors R31 to R36 added. R16 changed from 33 k to 27 k. D3, VT10, VT11, C6, C7 added. Incorporated at the same time as Modification No 3 Part B to Unit 1, Modification No 2 to Unit 14, Modification No 3 to Unit 4, Modification No 1 Part B to Unit 7, to reduce ripple on the -22 V drive to Unit 4 from the -41 V instabilised supply.

Modification No 2

38. Bracket H-33-1008-50 and diode SZ22BR removed and replaced by bracket H-33-1190-50 and diode BZY93C22, because original diode became obsolete.

Modification No 3

39. R32 changed to 1 k, to ensure satisfactory switching of the -22 V supply with high beta transistor VT7, VT10, VT11 and high leakage zener diode D1.

Modification No 4

40. R33 changed to 1.2 k, R32 changed to 1 k. Zener diode D2 moved to chassis for infinite heat sink. Incorporated to prevent over-dissipation of VT10 and to prevent over-dissipation of D2 under fault and test conditions.

PANEL FILTER SWITCHING, UNIT 12

Modification No 1

41. 47 pF capacitor connected between pins 8 and 3 of transformers T1 and T4. 270 pF capacitor connected between pins 1 and 6 of transformers T2 and T3. Incorporated to prevent spurious high frequency oscillations.

CABINET, R.F. RECEIVER 5820-99-519-7018

Modification No 1

42. Cable shortened and two cable ties added, to prevent cable harness leads fouling the cover flange.

Modification No 2

43. Two 0.01 µF capacitors connected between base and emitter, base and collector of VT2. Incorporated to prevent HF oscillations on the +30 V stabilised supply when transistors BD123 replace transistors BYD11.

Modification No 3

44. Bolt added on right hand wall of cabinet for earthing.

AMPLIFIER AUDIO FREQUENCY, UNIT 5

Modification No 1

45. Two 680 pF capacitors C45, C46 added, to prevent spurious r.f. oscillations.

TEST EXTENSION ELECTRONIC CIRCUIT PANEL, 16-WAY, M32-5264-01

46. This panel is at Modification state 0.

APPENDIX 1

SERVO AMPLIFIER USING CHOPPERS

CONTENTS LIST

	Paragraphs
Introduction	1, 2
Circuit Description	3 - 10

ILLUSTRATIONS

	Figure No
Typical chopper amplifier, Circuit diagram and waveforms	1A, B, C, D

APPENDIX 1

SERVO AMPLIFIER USING CHOPPERS

Introduction

1. The input to a servo amplifier is usually a d.c. error signal. The d.c. amplification of the error signal would entail complex circuitry to minimize variations in output due to thermal drift. Amplification by a.c. means is far more practical since drift has negligible effect on the output of the servo amplifier.

2. The Chopper is a convenient method of converting the d.c. signal input to an a.c. signal. The resultant a.c. signal has amplitude proportional to the magnitude of the d.c. signal and its phase dependent upon the polarity of the a.c. signal.

Circuit Description

3. There are several arrangements of transistor chopper circuits, one type is illustrated in Figure 1A.

4. Transistor VT1 acts as a switch shunting the d.c. signal. A 400 Hz squarewave input across the base and collector of VT1 performs the switching of the transistor by biasing it alternately from saturation to cut-off. The amplitude of the switching voltage is sufficiently high to ensure switching at all levels of d.c. input.

5. Consider a d.c. input to VT1 as represented by the waveform shown in Figure 1B. The positive-going switching pulses as shown in Figure 1C turn VT1 'on', reducing the output of the chopper across A-B to zero. Negative pulses switch VT1 'off' allowing the output across A-B to follow the d.c. signal for the duration of the pulse. The resultant output across A-B is represented by the waveform in Figure 1D.

6. R.F. filtering is carried out by R1, C1. To prevent hunting of the servo around the tune point, C2, R2 form a phase advance circuit. MR1 and MR2 limit the amplitude of signal applied to VT1.

7. A change in polarity of the d.c. input causes a phase change in the chopper output. It can be seen that when the d.c. input is positive the output is in phase with the 400 Hz switching signal, and when negative it is 180° out of phase. Reference to Figure 1D shows how the change occurs.

8. The chopper circuit employs silicon planar 'NPN' type transistors. The very low collector leakage current of this type of transistor and the reversal of emitter and collector leads serve to ensure minimum current flow when the device is cut off.

9. The output from A is capacitively coupled to the 400 Hz servo amplifier which converts the low level squarewave from the chopper into a 400 Hz sine-wave of sufficient amplitude to drive the motor.

10. In the circuit shown the d.c. input is isolated from earth by C3. In some cases one side is clamped to earth, so that C3 is not required.

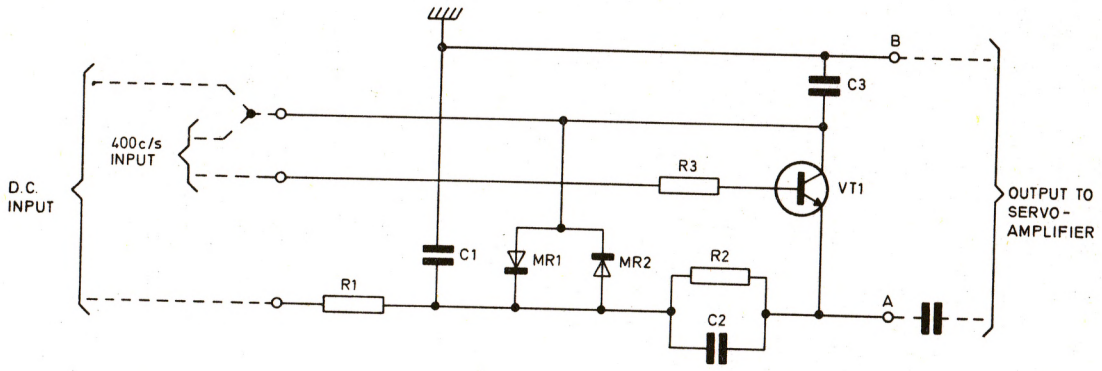


FIG. 1A CIRCUIT DIAGRAM

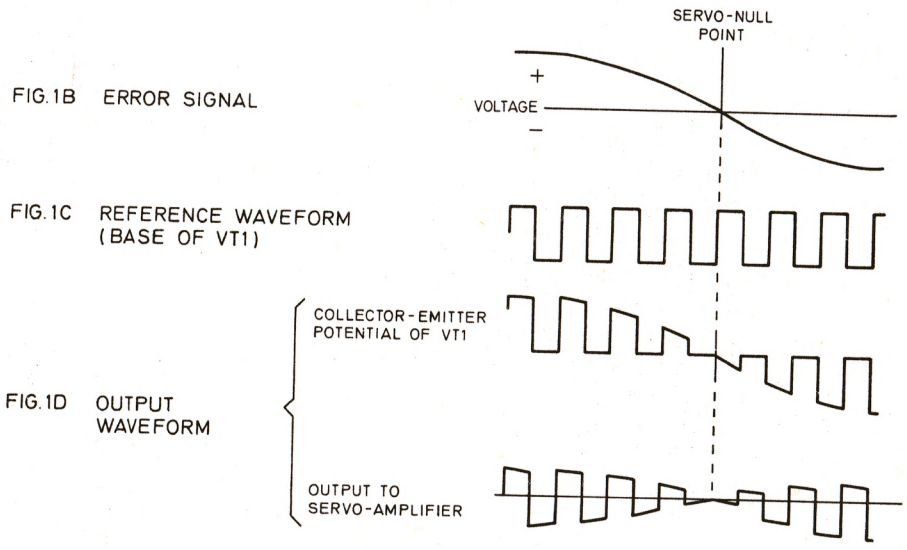


FIG. 1B ERROR SIGNAL

FIG. 1C REFERENCE WAVEFORM (BASE OF VT1)

FIG. 1D OUTPUT WAVEFORM

TYPICAL CHOPPER CIRCUIT AND WAVEFORMS

FIG. 1

PART 5B
SWITCHING ON/OFF AND SETTING-UP

CHAPTER 1

SWITCHING ON/OFF AND SETTING-UP

CONTENTS LIST

	Paragraphs
Introduction	1,2
Mains Transformer Connections	3,4
Synthesizer Check	5
Front Panel Controls	6–14
Switching On/Off	15,16
METERING Tests	17,18

TABLES

	Table No
MAINS TRANSFORMER CONNECTIONS	1.1
METERING TESTS	1.2

CHAPTER 1

SWITCHING ON/OFF AND SETTING-UP

CONTENTS LIST

	Paragraphs
Introduction	1,2
Mains Transformer Connections	3,4
Synthesizer Check	5
Front Panel Controls	6–14
Switching On/Off	15,16
METERING Tests	17,18

TABLES

	Table No
MAINS TRANSFORMER CONNECTIONS	1.1
METERING TESTS	1.2

CHAPTER 1

SWITCHING ON/OFF AND SETTING-UP

Introduction

1. The Receiver is used in Type 641 and Outfit CJM and is therefore set-up in the appropriate cabinet. In the following paragraphs it is assumed that the cabinet supplies and connections are correct and that the associated equipment is serviceable.

2. It is important that records are kept so that changes in performance can be observed and appropriate action taken.

Mains Transformer Connections

3. 14T1 has two 135 V primaries, tapped so that they can be connected to suit supplies from 100 V to 270 V as shown in Table 1.1.

4. Remove the Power Supply, Unit 14, release two screws which secure the hinged base plate and check that the connections are correct for the mains supply voltage.

TABLE 1.1

MAINS TRANSFORMER CONNECTIONS

Supply Voltage	Link		Connect Supply to	
	A to B		A	B
100	100	100	100	0
	0	0		
105	100	100	100	5
	5	5		
110	110	110	110	0
	0	0		
115	110	110	110	5
	5	5		
120	120	120	120	0
	0	0		
125	120	120	120	5
	5	5		
130	130	130	130	0
	0	0		
135	130	130	130	5
	5	5		

11. RECEIVE USB/DSB and RECEIVE LSB system switches are used to select appropriate detector, time constant and filter circuits for the supplementary characteristic of reception. SSB or DATA reception on LSB is independent of the usb channel except on DSB or MCW, when the lsb channel is inhibited.

12. USB/DSB or LSB output switches connect the appropriate sideband output to local or remote positions.

13. MONITORING switches connect the USB/DSB or LSB output to the loudspeaker and headsets. The loudspeaker will not monitor a transmitter side-tone.

14. The VOLUME control is for headset and loudspeaker.

Switching On/Off

15. To bring the Receiver into operation, proceed as follows:-

(1) Check that the RECEIVER fuse 1FS3 is correct for the mains supply voltage. It should be 1 A for 230 V, 2 A for 110 V.

(2) Check the neon indicator at the bottom left-hand corner of the cabinet to see that the mains supply is available.

(3) Switch the SUPPLY switch ON.

(4) Check that the SUPPLY, TUNING and CUTOUT lamps come on.

(5) Check that the SYNTHESIZER dials are illuminated.

(6) Check that the TUNING and CUTOUT lamps go out in about one second.

(7) Set the USB/DSB and LSB system switches to the type of reception.

(8) Check that when either system switch is moved from its OFF position the associated ON lamp comes on.

NOTE When the USB/DSB system switch is on DSB or MCW, the lsb channel is inhibited and its ON lamp will not light.

(9) Set the output switches to LOC, REM1 or REM2.

(10) Set the headset and loudspeaker MONITORING switches to USB/DSB or LSB.

(11) Set the frequency on the Synthesizer.

(12) Check that the TUNING lamp is on until tuning is completed, which should be in about one second.

(13) With the METERING switch to AGC position 16 or 17 (USB or LSB), adjust RF GAIN until the signal strength indicated on the meter starts to rise. Set RF GAIN 20 dB further on from this position.

(14) Adjust FINE TUNING.

(15) Switch the SQUELCH switches IN.

(16) Switch the MUTE switch ON.

16. To switch off, switch the SUPPLY switch OFF.

18. Except where stated, the Synthesizer can be set to any frequency. On positions 18, 19 and 20, set the USB/DSB system switch to DSB and RF GAIN to 20 dB.

NOTE Do not leave the METERING switch at any position marked in red.

18. Except where stated, the Synthesizer can be set to any frequency. On positions 18, 19 and 20, set the USB/DSB system switch to DSB and RF GAIN to 20 dB.

NOTE Do not leave the METERING switch at any position marked in red.

METERING Tests

17. To check that the Receiver is operating correctly proceed as follows:-

(1) Switch the Receiver ON.

(2) Turn RF GAIN fully clockwise to maximum.

(3) Switch SQUELCH switches OUT.

(4) Switch MUTE to OFF.

(5) Turn USB/DSB and LSB system switches OFF.

(6) Switch MONITORING switches OFF.

(7) Disconnect the antenna.

(8) Check that the meter reading for each position of the METERING switch is as shown in Table 1.1.

TABLE 1.2 METERING TESTS

METERING Switch to			Meter Reading		Remarks
Posn.	Title		Normal	FSD =	
1	1 MHz		35 to 100	1.5 V	
2	RANGE	(1	10 ± 3		0.240 to 0.525 MHz
		(2	20 ± 3		1.0 to 1.999 MHz
		(3	30 ± 3		2.0 to 3.999 MHz
		(4	40 ± 3		4.0 to 7.999 MHz
		(5	50 ± 3		8.0 to 15.999 MHz
		(6	60 ± 3		16.0 to 27.999 MHz
3	SUPPLIES	(+230 V	40 ± 4	500 V	
4		(+30 V	60 ± 4	50 V	
5		(-30 V	60 ± 4	50 V	
6	1K1 + 2		60 ± 9	48 mA	
7	FROM SYN	(37.5 MHz	> 2		
8		(VAR OSC	> 2		
9		(2.3 MHz	> 8		
10	FREQ. CH. DRIVES	(1st OSC	> 2		
11		(	50 to 80		Above 8 MHz)Varies with
		(3 MHz (	0		Below 8 MHz)frequency
12		(1.1 MHz	45 to 85		
13		(100 kHz	55 to 85		
14	AGC DET	(USB	< 10		
15		(LSB	< 10		
16	AGC	(USB	2 to 6		
17		(LSB	2 to 6		
18	IF TEST ON DSB	(	< 10		Below 8 MHz
		(4 MHz (	60 approx.		Above 8 MHz
19		(1 MHz	60 approx.		Below 8 MHz
20		(100 kHz	60 approx.		

TABLE 1.1 (Continued)

Supply Voltage	Link A to B		Connect Supply to A	Connect Supply to B
200	0	100	100	0
205	0	100	100	0
210	5	100	100	5
215	5	110	100	0
220	0	110	110	0
225	0	110	110	0
230	5	110	110	5
235	5	120	110	0
240	0	120	120	0
245	0	120	120	5
250	5	120	120	5
255	5	130	120	0
260	0	130	130	0
265	0	130	130	5
270	5	130	130	5

Synthesizer Check

5. On frequency ranges 1 to 4 the first oscillator drive is proportional to the level of the 2-3 MHz output from the Synthesizer to the Frequency Offset Unit at 1SKTAH. This level must be set as described under Frequency Synthesizer Check in Part 5C.

Front Panel Controls

6. The SUPPLY switch connects the mains supply to the Receiver and its associated Synthesizer.

7. FINE TUNING is used to clarify speech or to improve fst or data reception. It is normally set to 0.

8. R.F. GAIN controls r.f. and i.f. gain. It is marked from 0-120 to represent signal levels in dB above 1 V; shading to the left of 0 corresponds to the delay voltage required to produce A.G.C. The control is set about 20 dB above the A.G.C. threshold as in Paragraph 15, Step (13).

9. The MUTE ON/OFF switch connects or disconnects the external mute line. Normally ON to desensitise the Receiver when a transmission is made. It is switched OFF for duplex operation.

10. SQUELCH IN/OUT switches are used when receiving a strong SSB signal, to reduce background noise during signal pauses. It is normally ON.